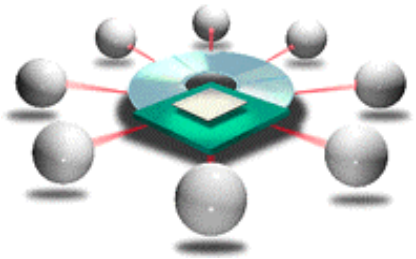
Xilinx Programmable Logic Design Solutions

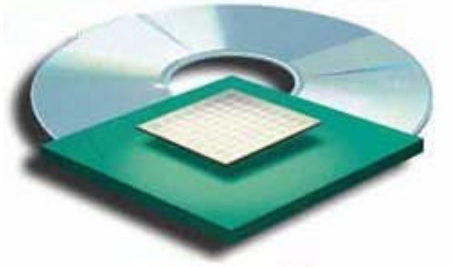
Version 2.1i

ALLIANCE Series Software



Designing the Industry's First 2 Million Gate FPGA

FOUNDATION Series Software



Drop-In 64 Bit / 66 MHz PCI Design

XILINX®

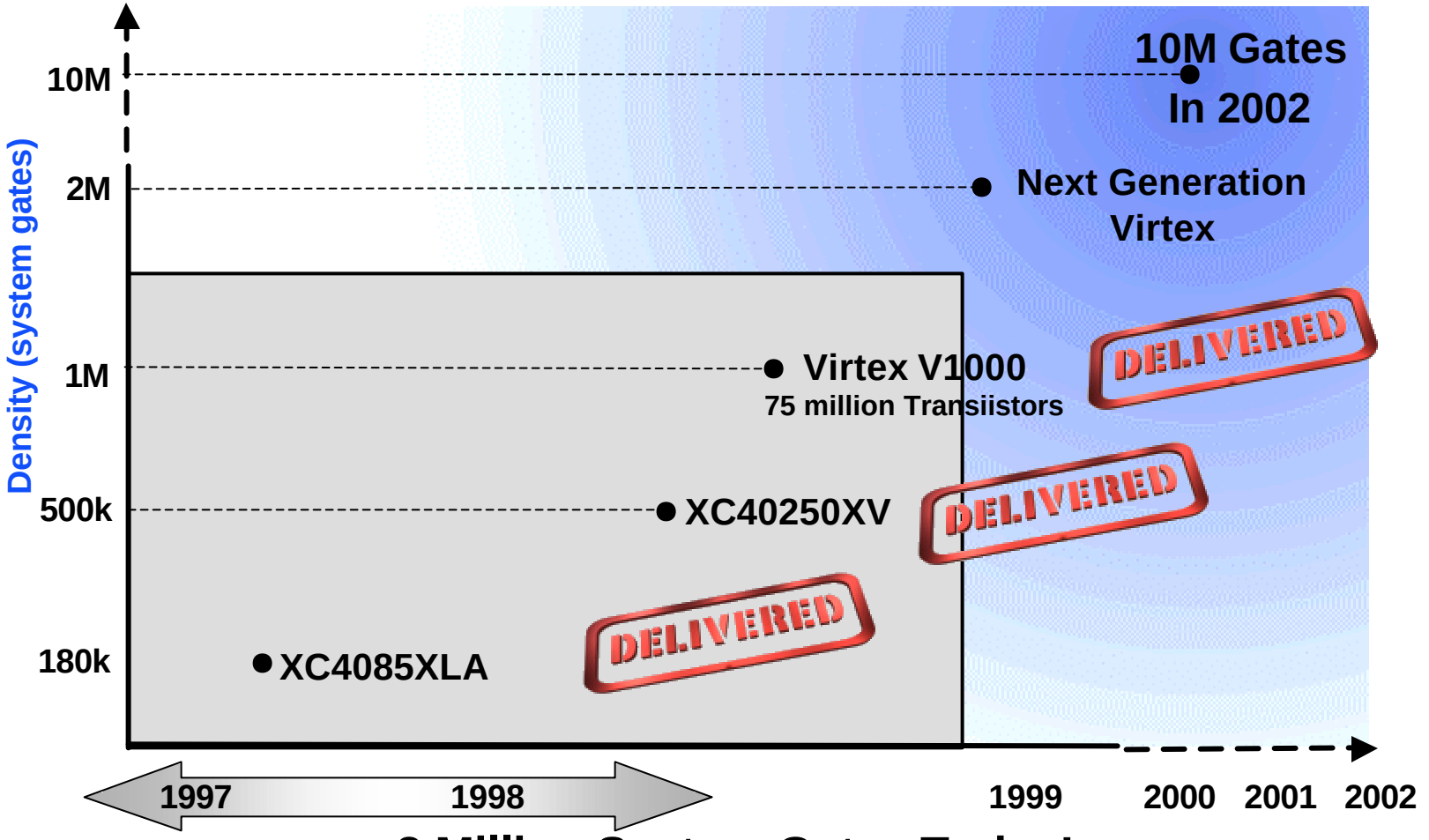
State of the Art Programmable Logic Design

- Industry's fastest compilation times
- Industry's highest performance
- Industry's best support for High-Level design flows
  - HDL design
  - Design re-use / Cores
  - Robust functional and timing verification
  - Internet enabled design

- Support for the industry's largest FPGAs
- Products configured to meet your design needs

XILINX®

Density Leadership



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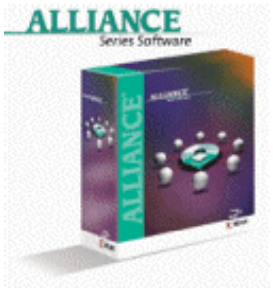
Software Leadership



DELIVERED

v1.5i **Ease Of Use**

- ✓ Push Button Design
- ✓ Minimum Delay Reporting
- ✓ Voltage/Temperature Prorating
- ✓ Floorplanning

DELIVERED

v2.1i **Internet Enabled Software**

- ✓ Internet Team Design
- ✓ 2 Million Gate support
- ✓ 100K Gates < 1 minute
- ✓ Embedded Core Generator
- ✓ Drop-In 64 bit / 66 MHz PCI

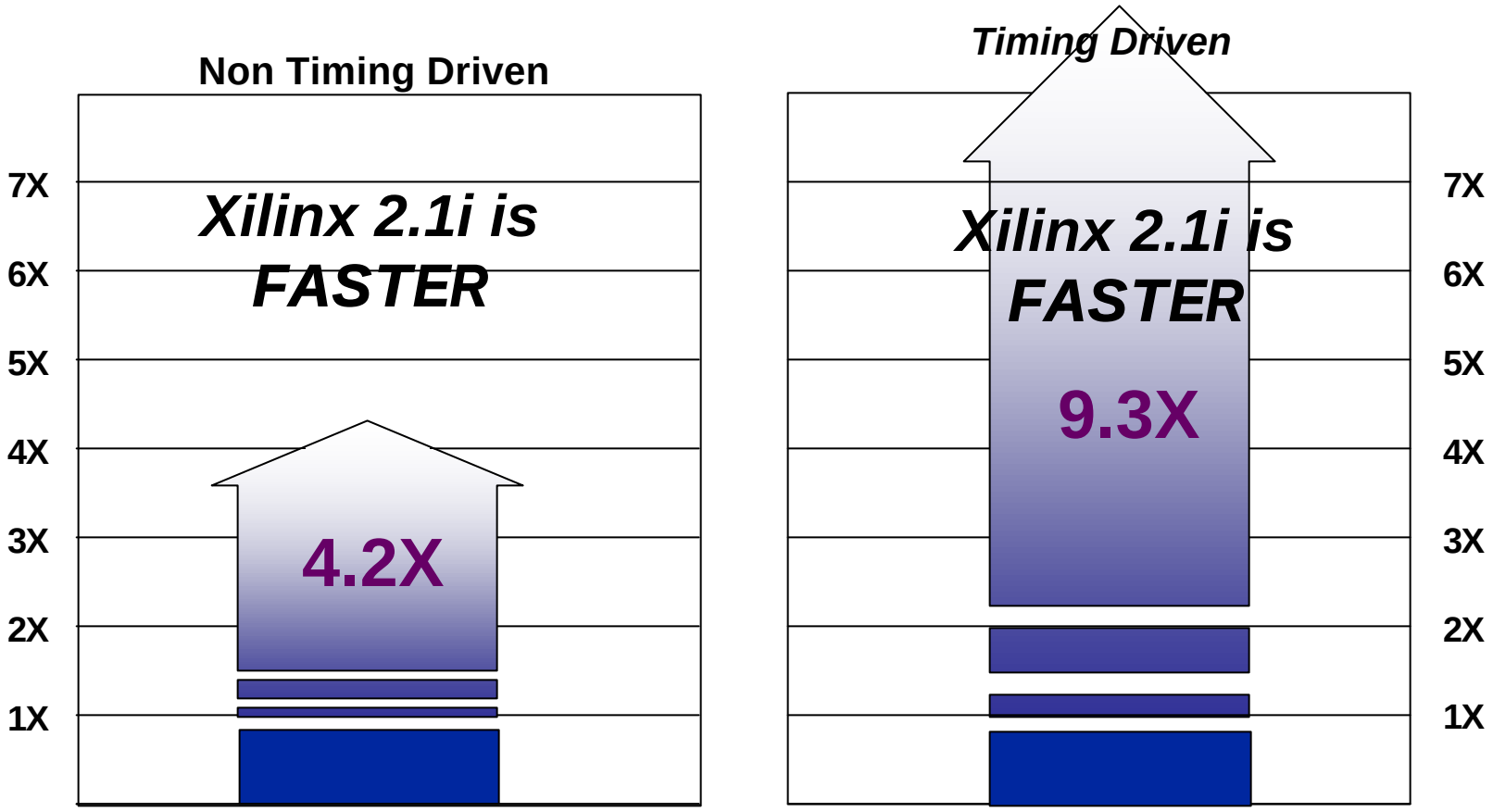
Xpresso

1998 1999

XILINX®

Benchmark Results

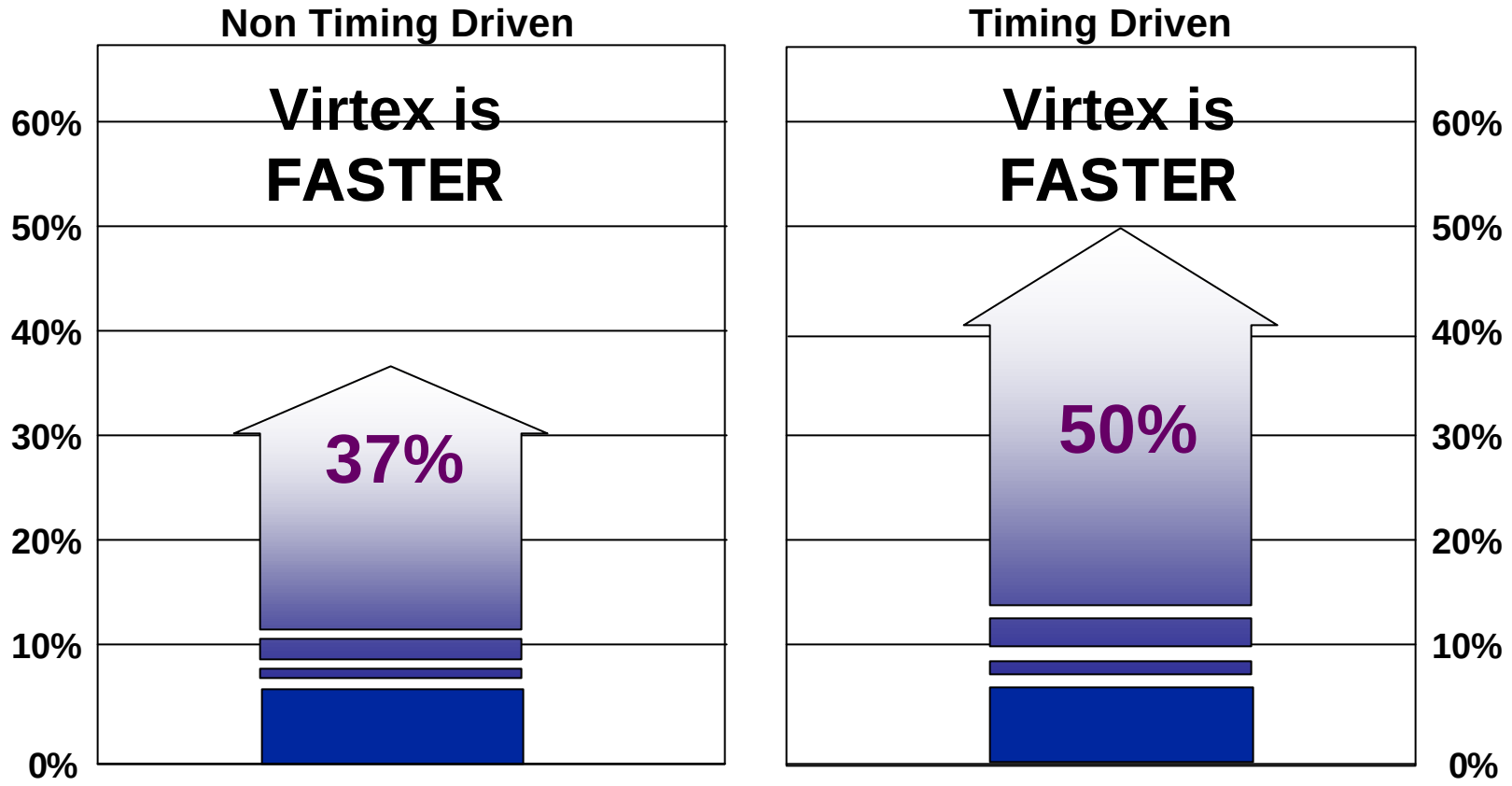
Virtex vs. 10KE Compilation Time



- Benchmarks are comparing Virtex -6 with 10KE-1 using Alliance version 2.1i vs. MAX+PLUS2 9.1
- Design suite consists of 22 HDL customer designs ranging from XCV50-XCV600

Benchmark Results

Virtex vs. 10KE Performance



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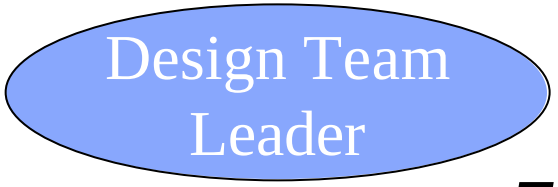
VIRTEX

XILINX®

Internet Team Design

Solves 21st Century Design Challenges

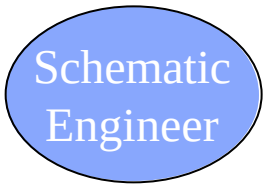


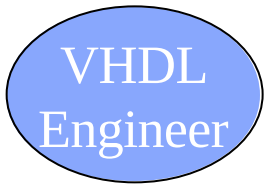
The Problem

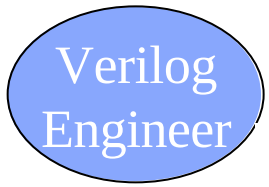
- Million+ Gate Designs
- Variety of Flows
- Remote Location of Designers
- Design Revision Management

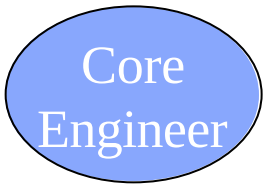
The Solution

- Communication
- Coordination
- Integration









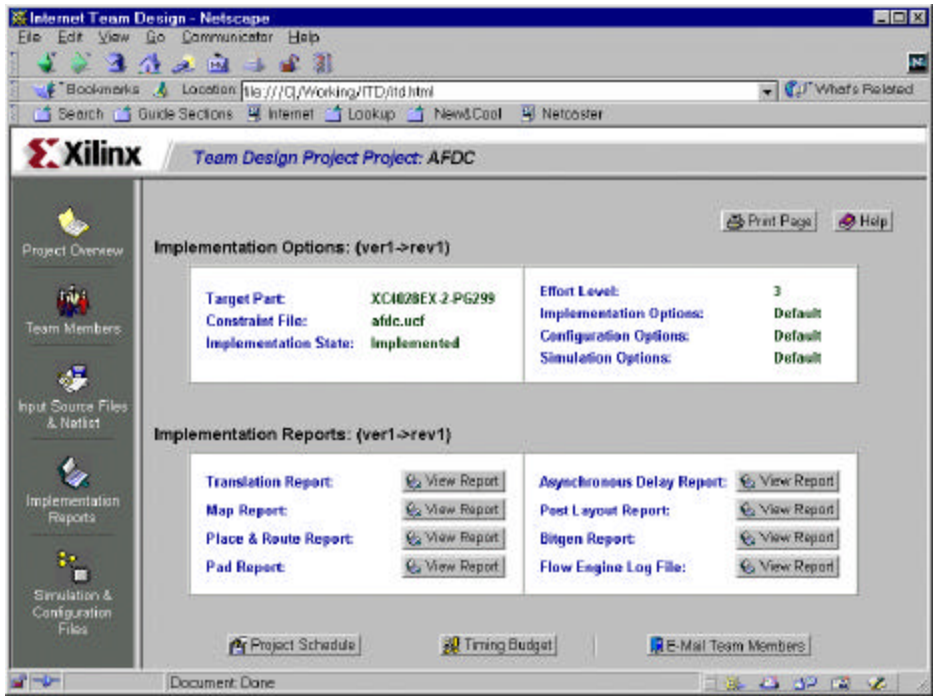
XILINX®

Internet Team Design
Product Description

A web-based facility to coordinate and manage team-based design projects

Key features include:

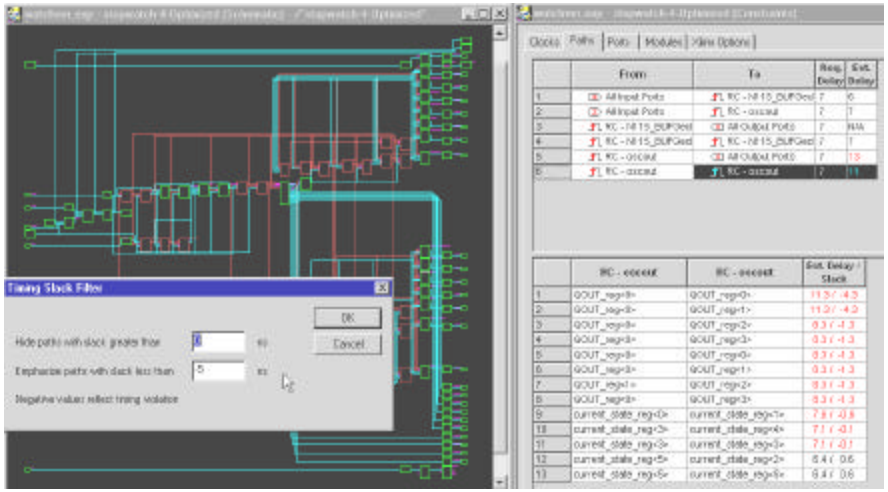
- Facilitates project schedule, assignments and communication among team members
- Coordination of input source and netlist files from multiple designers
- Provides access to implementation reports, timing simulation and configuration files



XILINX®

Synopsys
FPGA Express™ 3.2

- Push-Button HDL Performance:
  - Advanced synthesis delivers faster clock speeds, and more efficient utilization



- Powerful HDL design:
  - TCL scripting enables ASIC - style design flow
  - Advanced Analysis features simplify design debugging:
    - Integrated Schematic Viewing and Static Timing Analysis (VISTA™)
    - Consistent signal naming

XILINX®

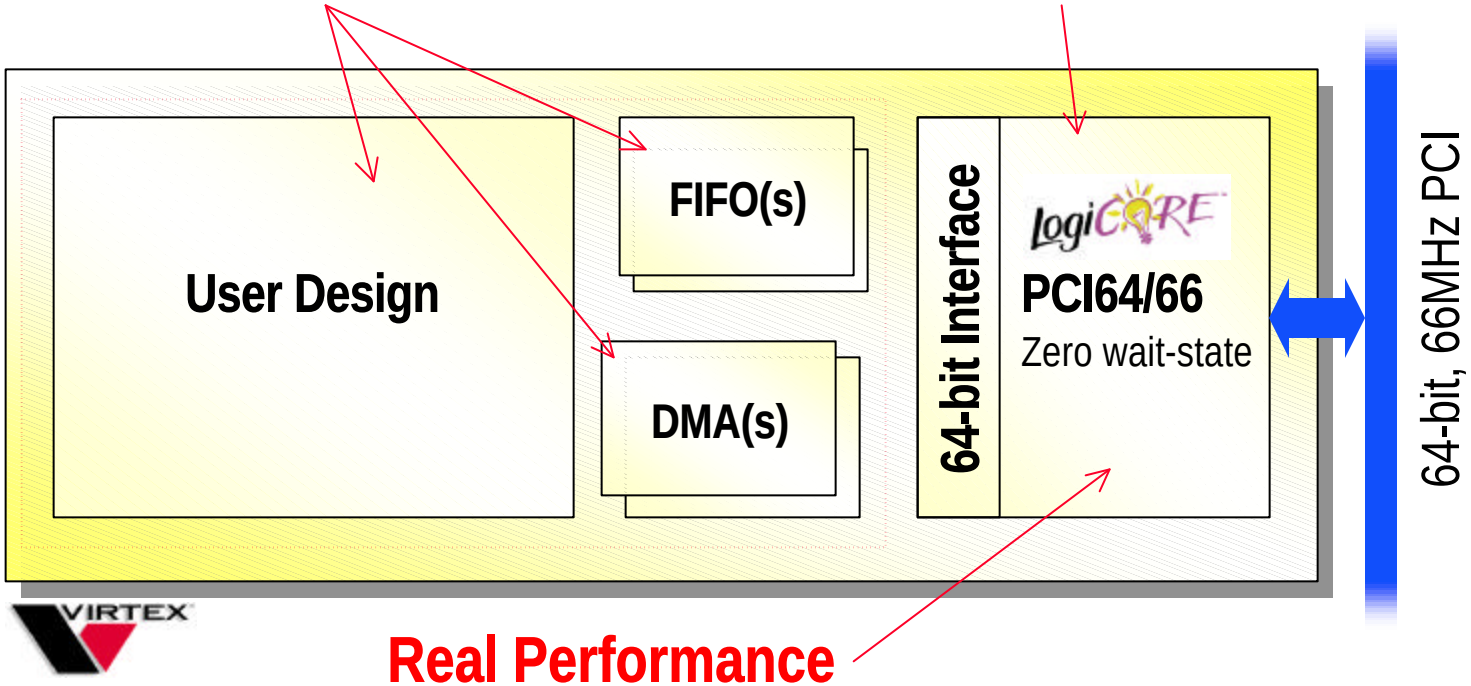
The Real 64/66 PCI

Real Flexibility

- Uses standard Virtex FPGA
- Back-end de-coupled from core

Real Compliance

- PCI v2.2 Initiator and Target
- Guaranteed timing



Real Performance

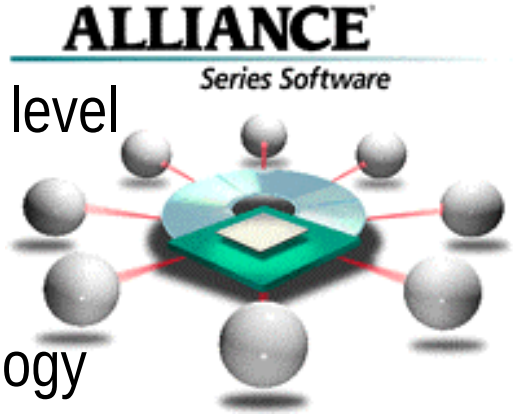
- Compliant zero wait-state at 66MHz
- Full 64-bit data path

XILINX®

Xilinx Alliance Series

Programmable Logic Design Tools Integrated Into Your EDA Environment

- Robust support for the complexities of multi-million gate FPGA design
  - High performance synthesis
  - Advanced design analysis through board level verification
    - STAMP and LMG models
- Industry's first Internet Team Design methodology
- Productivity enhancements speed system level design
  - Dramatic compile time improvements
  - Extensive IP
  - Design timing and layout analysis tools



XILINX®

Xilinx Foundation Series

A Complete, Ready to Use Programmable Logic Design Environment

- Easy to use, mixed-level design environment
  - Industry's fastest compilation times
  - Embedded core generation tool
  - Industry's most comprehensive on-line support
- Powerful, mixed-language synthesis from Synopsys®
- Drop-In PCI design
  - 64 bit / 66 MHz Virtex "Real PCI"
  - 32 bit / 33 MHz SpartanXL PCI