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FOR IMMEDIATE RELEASE

XILINX ANNOUNCES NEWEST MEMBER

OF INDUSTRY'S FASTEST GROWING CPLD FAMILY

New XC95144 device targets sweet spot of ISP CPLD market with lowest price per macrocell

SAN JOSE, Calif., May 6, 1998—Xilinx, Inc., (NASDAQ:XLNX), announced today it will begin volume shipments this month of the newest member of the 5-volt XC9500 family of aggressively priced CPLDs. The XC95144 device, with a 7.5 ns pin-to-pin speed, is the first member built on a new advanced process technology. This device completes the company's popular ISP family and, with 144 macrocells, it addresses the designers' needs in the density sweet spot of the CPLD market.

The XC95144 device is the first CPLD using an advanced FastFLASH process technology from United Semiconductor Corporation (USC), Taiwan. During 1998, all other members of the XC9500 family will be transitioned to this new process, which offers more than a 50 percent die size reduction compared to the initial 0.6-micron process. The die size reductions afford lower cost thereby allowing Xilinx to offer the lowest priced, high-performance CPLDs on the market.

"Offering our customers more efficiently engineered silicon on advanced process technology is paramount to our leading-edge technology strategy," said Evert Wolsheimer, vice president and general manager of the Xilinx CPLD division. "We are setting the price standard in the CPLD market with the lowest price per macrocell available from any CPLD vendor."

Customers spoiled by easy ISP

"The compelling design advantages of a mature in-system programmable technology combined with the promotional pricing of the Foundation Series tools made the change to Xilinx and the XC9500 CPLD family an easy choice. We've completed one design, a complex board with several XC9500 devices, and have started another project which will have multiple XC9500 devices per card," said Howard Katz, engineer, from Anatek,

Scottsdale, Ariz., a product design company providing related services. "The devices operate exactly as indicated in the specifications and we've been spoiled by the easy in-system programming!"

The new member completes the XC9500 CPLD family with densities ranging from 36 to 288 macrocells in a variety of packages. The XC9500 family features an architecture optimized for pin-locking, a necessity for designers who want to take advantage of in-system programming (ISP) for easier prototyping, simpler manufacturing, and remote equipment upgrades.

Industry's Best Value

Following suit on last year's price reductions, the XC95144 device is available at \$12.50 in 100-piece quantities in the 100-pin plastic-quad flat pack (PQFP) package, with high-volume quantities in mid-1999 priced at \$6.95. This represents the best cost-per-macrocell in the industry for a CPLD offering industry-leading ISP capabilities. The Xilinx Foundation Series software and third-party interfaces from the Xilinx Alliance Partner program fully support the entire XC9500 family.

Device		new				
	XC9536	XC9572	XC95108	XC95144	XC95216	XC95288
Macrocells	36	72	108	144	216	288
T _{PD} (ns)	5	7.5	7.5	7.5	10	15
Maximum						
User I/O	34	72	108	133	166	192
Packages	44VQFP	44PLCC	84PLCC	100TQFP	160PQFP	208HQFP
	44PLCC	84PLCC	100TQFP	100PQFP	208HQFP	352BGA
	48CSP	100TQFP	100TQFP	160PQFP	352BGA	
		100PQFP	160PQFP			

COMPLETE XC9500 SERIES

Xilinx is the leading innovator of complete programmable logic solutions, including advanced integrated circuits, software design tools, predefined system functions delivered as cores, and unparalleled field engineering support. Founded in 1984 and headquartered in San Jose, Calif., Xilinx invented the field programmable gate array (FPGA) and commands more than half of the world market for these devices today. Xilinx solutions enable customers to reduce significantly the time required to develop products for the computer, peripheral, telecommunications, networking, industrial control, instrumentation, high-reliability/military, and consumer markets. For more information, visit the Xilinx web site at www.xilinx.com.

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