The Xilinx Virtex™ Series:

Redefining FPGAs

A Product Backgrounder

Introduction

The new Xilinx Virtex series, now shipping, fundamentally redefines programmable logic by expanding the traditional capabilities of field programmable gate arrays (FPGAs) to include a powerful set of features that address system level problems for high performance designs. The Virtex series has numerous built-in features to solve designers' challenges throughout the system: broad capability for chip-to-chip communications through support for new I/O standards, clock signal synchronization on the FPGA and on the board, and a memory hierarchy to manage fast access to RAM on and off chip.

With the Virtex series, digital designers for the first time can use an FPGA to perform not only familiar logic functions, but also tasks that were formerly handled at the board level by separate, dedicated parts. The Virtex series eliminates the need for components such as phase lock loops, voltage translation buffers, and memory when on-chip RAM is sufficient. This high level of integration allows designers to reduce overall system power requirements, cut costs, and save board space.

Board-level functions supported by the Virtex series include multiple, fully digital delay locked loops (DLLs) and support for more than a dozen deep submicon signaling standards. With these and other unique features, the Virtex series has created a new industry benchmark for FPGA functionality and performance. The Virtex series has transformed the FPGA from its former role as a "glue logic" device into the industry's first programmable solution that can serve as the board-level center for system design.

Wide Ranging Technology Advances

The Virtex series continues more than a decade of innovation and technical leadership in programmable logic by Xilinx, and it marks the fourth generation of FPGA devices developed by the company since Xilinx introduced the world's first such device in 1984.

The culmination of four years of research and development, Virtex technology represents significant breakthroughs in several fields of programmable logic: semiconductor manufacturing processes, architecture, software design tools, and software cores. Xilinx has applied for more than 20 patents for inventions incorporated in Virtex technology.

Using beta software that has been available since November 1997, customers worldwide have been implementing designs on Virtex FPGAs, and several designs are nearing completion. Full production support for the Virtex series is now in version 1.5 of the Xilinx Foundation™ Series and Alliance ™ Series design and implementation tools, which began shipping earlier this year.

Scalable FPGA Platform

Virtex technology provides the foundation for a scalable platform of mainstream advanced 0.22 micron, five-layer metal FPGA devices operating at system frequencies of up to 160 MHz. Densities for the new Virtex FPGAs range from the Xilinx XCV50™ device, with 50,000 system gates at the low end, to the high-end Xilinx XCV1000 ™ device, the industry's first one-million gate FPGA. Xilinx began shipping the XCV1000 in October 1998.

The Virtex XCV1000 FPGA is the world's largest FPGA device and ranks as one of the most complex standard integrated circuits built to date, featuring approximately 75 million transistors. The Virtex XCV1000 doubles the density of programmable logic previously available to digital designers in the 500,000-gate Xilinx XC40250XV ™ device.

All of the initial nine members of the Virtex series are scheduled to be shipping in production volumes during the first quarter of 1999. The Xilinx Virtex series FPGAs are affordably priced and deliver more gates, higher performance, and unique features at a lower price than other FPGAs. Virtex pricing will start below $10 for 50,000 system gates. Prices are for 100,000-unit orders for delivery in late 1999. Packaging options for the Virtex series will include plastic quad flat packs (PQFP), ball grid arrays (BGA), 1.0-mm fine pitch BGA, and 0.8-mm chip scale package (CSP).

Virtex Device Offerings			
Virtex device	**Logic cells**	**System gates**	**Block RAM bits**
XCV50	1,728	57,906	32,768
XCV100™	2,700	108,904	40,960
XCV150™	3,888	164,674	49,152
XCV200™	5,292	236,666	57,344
XCV300™	6,912	322,970	65,536
XCV400™	10,800	468,252	81,920
XCV600™	15,552	661,111	98,304
XCV800™	21,168	888,439	114,688
XCV1000	27,648	1,124,022	131,072

Vast Routing Resources

The Virtex series features a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input-output blocks (IOBs), all interconnected with a highly efficient segmented routing structure. Five layers of metal provide a significant increase in routing resources over previous families of FPGAs. This reduces the interconnect delay and allows the Virtex series to accommodate very complex designs while delivering fast and predictable performance.

The Virtex CLB implements logic using four independent four-input lookup tables, four independent set/reset registers, multiplexer logic, and specialized arithmetic logic. The CLB was developed in parallel with the synthesis tools for the Virtex series to guarantee high performance results when used with VHDL and Verilog design methodologies. Complex logic such as 32-bit arithmetic functions, pipelined multiplication, and 64-to-1 multiplexing can be easily described in a high level language and will operate above 100 MHz in any Virtex device.

Foundation for Multi-million Gate Devices

Xilinx Virtex technology will allow the new series of system level FPGAs to migrate easily to the next generation 0.18-micron process that Xilinx is developing with its semiconductor fabrication partners. The 0.18-micron process will enable Xilinx to manufacture a Virtex FPGA device with two million system gates in the near future. High-end Virtex FPGAs are expected to compete with standard-cell application-specific integrated circuits (ASICs), while lower density Virtex devices are positioned to compete with mask-programmed gate array ASICs.

Dramatic Improvement in Design Productivity

For more than a decade, FPGAs have provided digital designers with continuously higher levels of logic density and performance while offering more flexibility and less risk than traditional ASICs. As a result, electronics manufacturers have been able to bring their products to market faster. The new Xilinx Virtex technology preserves this basic value of FPGAs, even for very high-density devices.

To leverage optimal use of the Virtex architecture, Xilinx focused its software efforts on the highest quality of synthesis results and very fast compile times. Implementation tools from Xilinx, and synthesis software from its leading EDA partners, were developed in tandem with the Virtex architecture to ensure high productivity for engineers who design with FPGAs. As a result, designers can expect timing-driven compile times of less than five hours for a one-million gate design—or about 200,000 gates an hour. This dramatic reduction in compile times is attributable to the vast routing resources of Virtex devices and to features such as an abundance of registers, latches, multiplexers, and carry logic.

All features of the Virtex architecture are accessible to designers who work with hardware description languages (HDLs) and who design at the register transfer level (RTL). Xilinx EDA partners such as Aldec, Cadence, Exemplar Logic, OrCAD, Model Technology, Mentor Graphics, Synplicity, Synopsys, and Veribest, all provide support for the Virtex series in their front-end design tools.

DLL for Advanced Clock Synchronization

As system performance requirements exceed 100 MHz, digital designers cannot tolerate long clock-to-output times, input set-up times, or on-chip clock skew. To solve this, the Xilinx Virtex devices offer four independent, fully digital delay locked loop circuits that allow internal and external clock synchronization. This capability removes clock skew from the entire system and delivers an increase in system performance up to 100 percent. Each DLL can lock on to a clock frequency up to 180 MHz and provide a variety of outputs that allow high precision in placing clock edges where required. Common applications for Virtex series DLLs include:

- The *zero-delay internal clock* for locking on to an external clock source, synchronizing clock edge that is external to the Virtex FPGA with the clock edge of a register inside the device. This provides clock-to-output delays of less than five nanoseconds.

- The *clock mirror* for using the Virtex Series DLL to lock on to a system clock and provide multiple synchronized clocks to the rest of the system. This is useful when interfacing to a system such as PCI that specifies a loading limit on the system clock. Combining prudent board design techniques with the Virtex Series DLL clock mirror gives designers the ability to synchronize clock edges system-wide.

- The *clock frequency doubler* for locking on and doubling an input frequency. This feature simplifies board design by allowing lower frequency signals to be routed on the board. For systems with logic on both clock domains, the edges of the 1X and 2X clock are aligned to avoid race conditions and mestability problems.

- The *clock phase synthesis* for generating 90º, 180º, and 270º phase shifts from an input frequency. This allows the system designer to move clock edges in a controlled way to meet specific setup, hold, and clock-to-output requirements.

SelectRAM+ ™ and Memory Hierarchy

For high-density designs, the demand for RAM increases at a greater rate than the demand for logic. The Virtex series is designed to connect with any amount of RAM through the Xilinx SelectRAM+ ä features.

- For bytes of RAM, Virtex FPGAs provide distributed SelectRAM ™. Pioneered in the Xilinx XC4000 ™ family, distributed SelectRAM is the use of the Virtex CLB lookup table resources as 16 x 1 static memory elements.

- For kilobytes of memory required in such applications as ATM buffers, video line buffers, and data-path FIFOs, Xilinx has introduced Virtex block SelectRAM+ memory. Each block of SelectRAM+ memory is a highly configurable, 4096-bit block of dual-ported synchronous SRAM. Each port can be configured to a variety of depths and widths ranging from 4096 x 1 to 256 x 16. Five-nanosecond clock-to-output and 1.2-

nanosecond address setup times allow over 160 MHz burst performance from these elements. Each port can be configured for independent width and depths. A typical application for this flexibility is to minimize device I/O requirements. Data buffers can interface to external logic at a high data rate while operations on the data can be performed on wider busses internally. Combined with the clock doubling capability of the Virtex DLL, implementing such a buffer is an easy task for designers.

- For high bandwidth access to megabytes of fast memory off chip, Virtex devices are capable of interfacing directly with SSTL and HSTL logic levels used by high-speed memory devices, as described in the following section.

Virtex SelectI/O ™

In recent years, a large number of new and specialized signaling standards tailored for specific applications have emerged, each with its own specifications for current, voltage, and termination techniques. The Virtex series addresses this problem by building configurable I/O structures that can interface to many different standards. These include Stub Series Transceiver Logic (SSTL) and High Speed Transceiver Logic (HSTL) to connect with fast 3.3-volt and 2.5-volt memories, and the Advanced Graphics Port (AGP) to interface with the Intel Pentium II processor for graphics applications.

The Virtex series also supports the Gunning Transceiver Logic (GTL and GTL+) I/O standards designed to interface with high performance microprocessors and backplanes. The Virtex SelectI/O feature also supports high-speed busses such as PCI33 and PCI66, which require specific current versus voltage characteristics.

These I/O standards solve performance issues, but some of them require specialized output and input buffers on the board. With the Virtex series, up to eight different voltage and signal standards can be directly connected to a single Virtex device.

Direct interfacing with these I/O standards eliminates the need for external buffers, increases performance, cuts costs, and reduces board space. Virtex SelectI/O supports the following bus standards:

LVTTL	HSTL Class I	SSTL2 Class 1
LVCMOS2	HSTL Class III	SSTL2 Class II
PCI	HSTL Class IV	CTT
GTL	SSTL3 Class I	AGP

GTL+ SSTL3 Class II

Virtex Core Methodology

The Virtex series extends the Xilinx Smart-IP technology first available on the XC4000 family of FPGAs. The vector-based interconnect structure of the Virtex series further extends the suitability of FPGAs to take advantage of the Xilinx high performance, highly predictable, and easy to use core methodology. Based on an abundance of routing resources of various lengths, the vector-based interconnect structure allows more cores with higher performance requirements to be implemented in HDLs than were possible in older architectures. Smart-IP ™ technology allows the core designer to leverage the absolute maximum performance for the fastest cores without giving up predictability or ease of customization. IP core developed with Xilinx Smart-IP technology are unique because they maintain their performance and predictability regardless of the size of the device in which they are implemented, or the number of cores used in a device.

Cores Available for Virtex Series

Building blocks	Complex cores	Memory
Multiplexers	Filters	Asynchronous FIFO
Counters	Reed Solomon - encoder	Synchronous FIFO
Registers	Reed Solomon - decoder	DMA controller
Adders/Subtractors	HDLC	Dual port block RAM
Accumulators	622 Mbits/sec SONET	Single port block RAM
Shift registers	JPEC encoder	
Comparators	Video streaming core	
Complementors	SDRAM controller	
	UART	
	82xx cores	

Summary

With advanced features such as thermal management, SelectI/O, support for multiple types of fast and unlimited memory, multiple digital delay locked loops, and a scalable architecture designed to support

fast software compile times and easy implementation of cores, the new Xilinx Virtex series clearly sets a new standard for mainstream FPGA design for the next century.

For more detailed information on the Xilinx Virtex series, including data sheets and applications notes, visit the product section of the Xilinx website at www.xilinx.com.

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