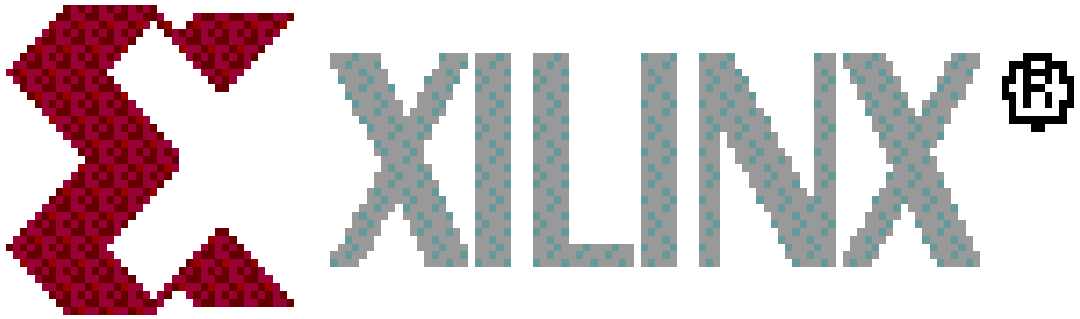
XILINX

Radiation Hardened FPGAs

The XQR4000XL Family

- 3 Device Sizes
  - XQR4013XL (10K to 30K system gates)
  - XQR4036XL (20K to 65K system gates)
  - XQR4062XL (40K to 130K system gates)
- Packages
  - Ceramic QFP - CB228
  - PQFP, BGA under consideration
- Temperature Range -55°C to +125°C

  Speed Grade
  - --3 over Military Temperature Range
  - ~ -1 over Commercial Temperature Range

XQR4000XL Radiation Specifications

- **Total Ionizing Dose**
  - **60K Rads**
- **Latch-up Immune**
  - **LET_{th} >100 MeV*cm²/mg @ +125°C**
  - **0.35m (drawn) epitaxial CMOS process**
- **Soft Upset Rate (upsets/bit-day)**
  - **2.43E-8 (Galactic p+)[1]**
  - **9.54E-8 (Galactic Heavy Ion) [1]**

Note1: For Low Earth Orbit (LEO), 680 km, 98° inclination, 100 mils Al shielding

IC Process

- 0.35µm epitaxial CMOS process
  - Thin, high quality gate oxide
  - Highly doped field oxide
  - Field implant in SRAM area
  - 7µm epi substrate
- Manufactured on QML Line
- QA Lot Monitor to insure Radiation Specifications

Xilinx/Lockheed Test
May 1998

- **XQR4036XL devices**
  - **0.35m (drawn) CMOS**
  - **Thin, high quality gate oxide**
  - **Highly doped field oxide**
  - **0.7m epi substrate**
- **Total Dose: 60,000 Rads**
- **Heavy-ion tests**
  - **LETs up to 120 MeV-cm^2/mg.**
- **Not a single case of latch-up @ 125 ^{o}C**

Calculated Upset Rates for LEO

Galactic H.I.	Galactic p+	Trapped p+	90% w/c p+	ALSF p+	90% w/c H.I.	ALSF H.I.
(ups/bit-day)	(ups/bit-day)	(ups/bit-day)	(ups/bit)	(ups/bit)	(ups/bit)	(ups/bit)
9.54E-8	**2.43E-8**	**2.50E-7**	**2.78E-6**	**1.78E-4**	**1.46E-6**	**1.44E-6**

Notes

1. Low Earth Orbit (LEO), 680 km, 98° inclination, 100 mil Al shielding
2. Heavy ion testing was performed on Xilinx XQR devices at Brookhaven National Laboratories. This data was used to calculate upsets from the galactic cosmic and solar flare environments
3. Space Radiation 2.5 and CHIME models were used for the galactic and solar flare conditions.
4. Space Radiation 2.5 was used for the trapped radiation and proton contribution from the flares.

Calculated Upset Rates for GEO

Galactic H.I.	Galactic p+	Trapped p+	90% w/c p+	ALSF p+	90% w/c H.I.	ALSF H.I.
(ups/bit-day)	(ups/bit-day)	(ups/bit-day)	(ups/bit)	(ups/bit)	(ups/bit)	(ups/bit)
2.34E-7	**5.62E-8**	**-**	**3.90E-6**	**2.49E-4**	**7.20E-6**	**6.98E-6**

Notes

1. Geostationary Earth Orbit (GEO), 35,000 km, 0° inclination, 100 mil Al shielding
2. Heavy ion testing was performed on Xilinx XQR devices at Brookhaven National Laboratories. This data was used to calculate upsets from the galactic cosmic and solar flare environments
3. Space Radiation 2.5 and CHIME models were used for the galactic and solar flare conditions.
4. Space Radiation 2.5 was used for the proton contribution from the flares.

Ericsson/SAAB test January 1998

- **XC4010 and XC4010XL**
  - Neutron single-event-upset tests at up to 100 MeV
  - Not a single case of latch-up
- **Conclusion**
  - SEU cross sections of 1.3 to 4.4 10^{-15} cm^2/bit
  - an order of magnitude below the lower limit reported for SRAMs
- **MTBF for avionics applications (at 10 km altitude,60^o N)**
  - 1,300,000 flight hours for the XC4010E
  - 275,000 hours for the XC4010XL

Ericsson Saab Avionics Conclusion

“SRAM-based FPGAs (Xilinx XC4000 series) show a low susceptibility to single event upsets caused by high energy neutrons …… we conclude that these SRAM - based FPGAs can be used without limitation in the atmospheric radiation environment, contrary to large SRAM memories where precaution in the use is necessary because of neutron-induced SEU.“

FPGA Configuration Memory

- Distributed Dual Port Memory
  - configuration/readback port
  - control “port”
- FPGA Functionality Defined by the State of the Memory
  - all bits “read” continuously
- Memory Loaded on Power-Up
  - can load itself
  - can be loaded by another

FPGA Configuration Memory (cont.)

- Memory Can Be Re-Loaded
  - at any time
  - any number of times
- Memory Can Be Read Back
  - during circuit operation
  - includes the “state” of the circuit

Inherently-Robust Latch Design

- Cross-coupled inverters plus write (read) transistor
- Common power and ground contacts
- Stability is equivalent to 6-transistor SRAM cell
  - active pull-up and pull-down
  - each ~5 kilohm on-resistance
- Typical 4-transistor SRAM cell uses polysilicon pull-ups
  - six orders of magnitude weaker
  - 5 gigohms vs. 5 kilohms

All Latches are Sensitive to Single-Event Upsets

- **Xilinx FPGAs store logic and routing in latches**
- **Antifuse-based FPGAs use fewer latches**
  - **only for user data, not for logic and interconnect**
- **All latches require some kind of error correction**

Xilinx FPGAs offer a unique, efficient way to correct SEUs

Rad-Hard Configuration Memories

E^2PROM

- Northrop Grumman (formerly Westinghouse, Baltimore)
- W28C64 -- 64K (8K x 8)
- W28C256 -- 256K (32K x 8)
- SEU LET_{th}
  - 60 MeV-cm^2/mg (read cycle)
  - 35 MeV-cm^2/mg (write cycle)

SRAM

- Honeywell
- HLX6228 -- 1M (128K x 8)
- $<1x10^{-10}$ Upsets/bit-day (Geosynchronous Orbit)