Single-Port Block Memory for Virtex™ and Virtex™-II V3.0

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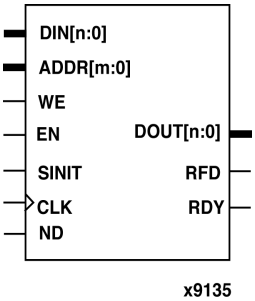

Figure 1: Core Schematic Symbol

Features

- Fully synchronous drop-in modules for Virtex™ and Virtex™-II families; uses Virtex and Virtex-II block memory for performance and efficiency
- Supports all three Virtex-II write mode options: Read-After-Write, Read-Before-Write; No-Read-On-Write. (Only available for Virtex-II implementation)
- Supports ROM and RAM functions
- Supports data widths from 1 to 256 bits
- Supports memory depths from 2 to 256K words for Virtex and from 2 to 1M words for Virtex-II.
- Available in the Xilinx CORE Generator™ System V3.1i

Functional Description

The Single-Port Block Memory module is generated based on the user-specified width and depth. This module for Virtex is composed of single or multiple Virtex 4Kb blocks called SelectRAM+. The Virtex-II Single Port Block Memory module on the other hand is composed of single or multiple 18Kb blocks called SelectRAM-II.

When the Block Memory is enabled, all memory operations occur on the rising edge of the clock input (CLK). When the block memory is disabled (enable inactive), the memory configuration and output value remain unaltered.

During a write operation (WE asserted), the data presented at the port's data input is stored in memory at the location selected by the port's address input. During this operation, the data output port behaves differently for the Virtex and Virtex-II architecture.

The Virtex implementation supports a single write mode option, Read-After-Write. This write mode causes the data being written to the addressed memory location to be transfered to the data output port when a write operation occurs.

The Virtex-II implementation supports three different "write mode" options that determine the behavior of the data output port (read port) during a write operation. The three options are (1) Read-After-Write (Write First), (2) Read-Before-Write (Read First), and (3) No-Change-On-Write (No Change).

During a read operation for Virtex implementation, the memory contents at the location selected by the address will appear at the module's output. When Synchronous Initialization (SINIT) is active, the module's registered outputs are synchronously reset to zero for Virtex and to a user-defined value for Virtex-II. The Synchronous Initialization command has no effect on the contents of the memory or write operations.

The initial contents of the memory (*i.e.,* the data stored in the memory immediately after device configuration) can also be specified.

For additional information on Virtex and Virtex-II Block Memory features, please refer to the *Virtex or Virtex-II Handbook* available at the website: http://www.xilinx.com/products/virtex/v2handbook.htm.

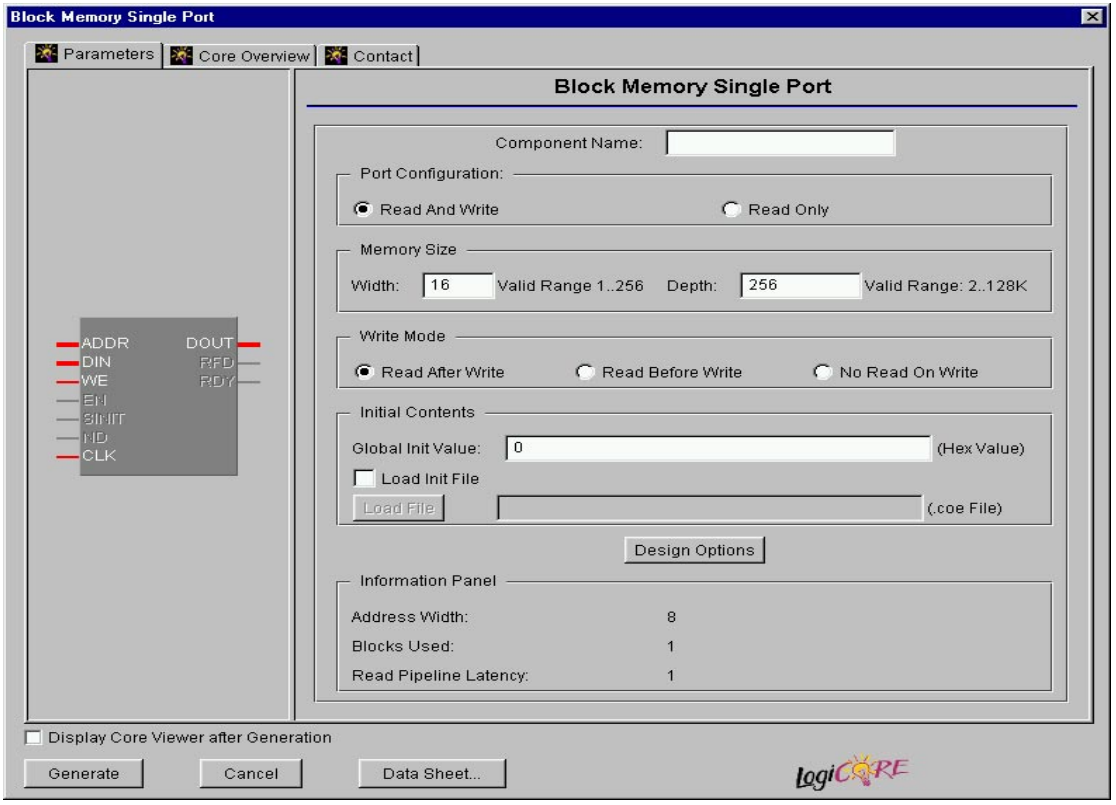

Figure 2: Single-Port Block Memory Main Parameterization Window

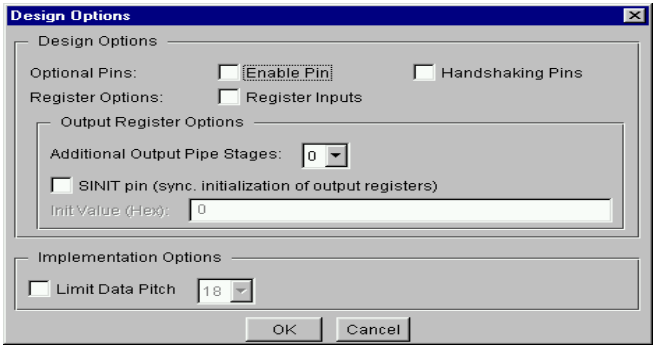

Figure 3: Single-Port Design Options Window

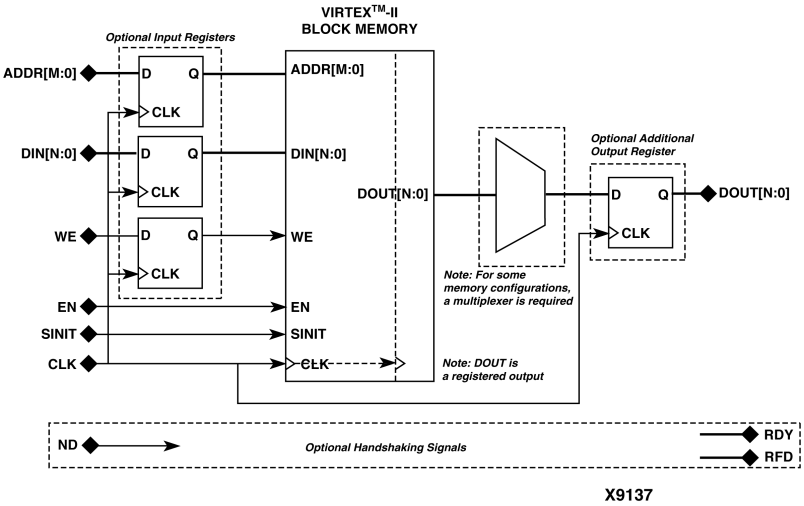

Figure 4: Single-Port Memory Block Diagram

Table 1: Core Signal Pinout

Signal	Direction	Description
DIN[n:0] (optional)	Input	**Data Input**: data written into memory.
ADDR [m:0]	Input	**Address**: memory location for data written to/read from.
WE (Optional)	Input	**Write Enable**: allows data transfer into memory (Active High).
EN (Optional)	Input	**Enable**: enables access to memory via read and write operations (Active High).
SINIT (Optional)	Input	**Synchronous Initialization**: forces module outputs to a predefined state.
CLK	Input	**Clock**: all memory operations synchronous with rising edge of clock input. When memory is enabled, all control signals, input/output data are registered on the rising edge of clock.
ND (Optional)	Input	**New Data**: indicates new and valid address on ADDR (Active High).
DOUT[n:0]	Output	**Data Output**: synchronous output of the memory.
RFD (Optional)	Output	**Ready for Data**: indicates that memory is ready for new address (Active High).
RDY (Optional)	Output	**Ready for Data**: indicates valid data on DOUT port (Active High).

Pinout

Port names for the core module are shown in Figure 1 and described in Table 1. The inclusion of some ports on the module is optional; excluding these ports will alter the function of the module. The optional ports are designated in Table 1. For additional information on Virtex or Virtex-II Block RAM, refer to the *Virtex or Virtex-II Handbook* available at the website: http://www.xilinx.com/products/virtex/v2handbook.htm.

Clock - CLK

Block Memory is fully synchronous with the clock input. All input pins have setup time referenced to the port CLK pin. The DOUT port has a clock-to-out time referenced to the CLK pin.

Enable - EN

The enable pin affects the read, write, and SINIT functionality of the port. When the Block Memory has an inactive enable pin, the output pins are held in the previous state and writing to the memory is disabled.

Write Enable - WE

Activating the write enable pin enables writing to the memory locations. When active, the contents of the DIN bus is written to memory at the address pointed to by the ADDR bus. The output latches are loaded or not loaded according to the write configuration (Write First, Read First, No Change). When WE is inactive, a read operation occurs, and the contents of the memory addressed by the ADDR bus are driven on the DOUT bus. In the Read Only port

configuration (ROM configuration), the WE pin is not available.

Synchronous Initialization - SINIT

When enabled, the SINIT pin forces the data output latches to synchronously load the predefined SINIT value. For the Virtex implementation, the SINIT value is zero. Therefore, asserting the SINIT pin causes the output latches to reset. For the Virtex-II implementation, the SINIT value is defined by the user. Consequently, asserting the SINIT pin causes the output latches to contain the user-defined SINIT value. This operation does not affect memory locations and does not disturb write operations. Like the read and write operation, the SINIT function is active only when the enable pin of the port is active.

Address Bus - ADDR[m:0]

The address bus selects the memory location for read or write access.

Data-In Bus - DIN[n:0]

DIN bus provides the data value to be written into the memory. Data input and output signals are always buses; that is, in a 1-bit width configuration, the data input signal is DIN[0] and the data output signal is DOUT[0]. In the Read Only port configuration (ROM configuration), the DIN bus is not available.

Data-Out Bus - DOUT[n:0]

The DOUT bus reflects the contents of memory locations referenced by the address bus during a read operation.

During a write operation of a Virtex memory (Read First configuration), the DOUT buses reflect the stored value before the write.

During a write operation of a Virtex-II memory (Write First or Read First Configuration), the data-out bus reflects either the DIN bus or the previously stored value before write. During a write operation in No Change mode, the data-out bus is not affected.

New Data - ND

Indicates that there is a new and valid address on ADDR Port.

Ready for Data - RFD

Indicates that the memory is ready to accept a new address. RFD is always true, except when EN is inactive.

Output Ready (Valid) - RDY

Indicates valid output on the DOUT port. RDY will lag ND by the latency of the block memory.

CORE Generator Parameters

The CORE Generator parameterization window for this module is shown in Figure 2 and Figure 3. The window shown in Figure 2 allows the memory ports to be defined. An information window, which is useful in verifying that the total number of blocks required does not exceed those available on the targeted device, is also shown at the bottom. The window shown in Figure 3 allows configuration of the design options. The available options are described below.

Definition of GUI Interface Fields

- **Component Name**: Enter a name for the output files generated for this module (up to 256 characters).
- **Port Options**:
  - **Width**: Select the data bit width. The width values can be between 1 and 256. Cores should not exceed the number of Block RAM primitives available in the targeted device.
  - **Depth**: Enter the number of words in the memory. The range of values is 2 to 262,144 (256K) for Virtex. The range of values is 2 to 1,048,576 (1M) for Virtex-II. The absolute maximum number of words is 1M for Virtex-II. Blocks used should not exceed the number of Block RAM primitives available in the targeted device.
- **Port Configuration**: Select one; the default is Read and Write.
  - **Read and Write**: Configured as Random Access Memory (RAM).
  - **Read Only**: Configured as a Read Only Memory (ROM).
- **Write Mode**: Select one for Virtex-II architecture. The default is Read-After-Write. The Virtex architecture supports only Read-After-Write.
  - **Read after Write**:
  - (1) No Inputs or Outputs Registered: The input data is transferred onto the DOUT port on the rising clock edge immediately following the assertion of the WE input.
  - (2) With Inputs Registered Only: The input data is transferred onto the DOUT port on the second rising clock edge immediately following the assertion of the WE input.
  - (3) With Outputs Registered: The input data is transferred onto the DOUT port on the second rising clock edge immediately following the assertion of the WE input.
  - (4) With Inputs and Outputs Registered: The input data is transferred onto the DOUT port on the third rising clock edge immediately following the assertion of the WE input.
  - **Read before Write**:
  - (1) No Inputs or Outputs Registered: The current data in the addressed memory location is transferred

onto the DOUT port on the rising clock edge immediately folowing the assertion of the WE input.
  - (2) With Inputs Registered: The current data in the addressed memory location is transferred onto the DOUT port on the second rising clock edge immediately following the assertion of the assertion of the WE input.
  - (3) With Outputs Registered: The current data in the addressed memory location is transferred onto the DOUT port on the second rising clock edge immediately following the assertion of the WE input.
  - (4) With Inputs and Outputs Registered: The current data in the addressed memory location is transferred onto the DOUT port on the third rising clock edge immediately following the assertion of the WE input.
  - **No Read on Write**: A write operation has no effect on the content of the DOUT port. The DOUT port is updated when WE is inactive.
- **Initial Contents**: Enter the parameter fields related to the data stored in the memory directly after device configuration.
  - **Global Init Value**: Enter the value to be stored in any memory location not specified by any other means. When no values are entered, this field defaults to 0. Value must be in Hex.
  - **Load Init File**: Selects the initial contents of the memory to be read from a *coe* file.
  - **Load File**: Press this button to activate a browser window that lets the user pick a coefficient or *coe* file that contains the initial contents of the memory. This is an ASCII file with a ".coe" extension. For further information regarding the memory's initial contents, refer to the *Specifying Memory Contents* section.
- **Design Option**: Press this button to display the design options dialogue box on the screen. The resulting display is shown in Figure 3.
- **Information Panel**: Window provides feedback on the memory based on the selected parameter values.
  - **Address Width**: Shows the number of bits needed to address all of the words in the memory.
  - **Blocks Used**: Shows the number of Block RAM primitives required to implement the specified Memory Depth and Width.
  - **Read Pipeline Latency**: Calculates the latency from the address port (ADDR) to the data output port (DOUT).
- **Generate**: Select to generate the block memory module. Make sure that the parameters are correctly selected for the particular application before executing this option.
- **Cancel:** Select to close window and return to the Core Generator.
- **Datasheet:** Select to generate a PDF version of this document.

Design Options

- **Optional Pins**:
  - **Enable Pin**: Check the box to include the enable port on the module; uncheck the box to remove it. This port provides an enable for all memory read and write operations. When it is inactive, the memory is disabled.
  - **Handshaking Pins**: Check the box to include the following ports; uncheck the box to remove them.
    - **ND** [New Data]: Signals a new and valid memory address whenever active. This port has no effect on the memory read and write operations. ND is valid only when RFD is active.
    - **RFD** [Ready For Data]: Indicates that the memory can accept new addresses. Always active when the memory is enabled.
    - **RDY** [Output is Ready]: Indicates to the user that the data on the output is valid. RDY will lag ND by the latency of the module.
- **Register Options**:
  - **Register Inputs**: Check this box to register ports DIN, ADDR, and WE prior to accessing block memory. See Figure 4.
- **Output Register Options**:
  - **Additional Output Pipe Stages**: Select "1" to enable an additional register on the output of the memory; select "0" to disable an additional register on the output of the memory. See Figure 4.
  - **SINIT PIN**: Check box to add the synchronous port SINIT to the memory. When this signal is active, the output of the memory is set to a predefined value. Enabling this port has no effect on the contents of the memory.
    - **SINIT Value** (HEX value): Enter the HEX value that the output port will get set to when the SINIT port is true. For Virtex implementation, this value is fixed to zero and cannot be altered.
- **Implementation Options**:
  - **Limit Data Pitch**: Select to limit the data pitch (or data width) of each of the RAM Blocks used to implement the memory. This optimizes the routing implementation of the block memory. Data pitch can be set to 8 or 16 for Virtex and 18 or 36 for Virtex-II.
- **Close**: Select to close window and return to main parameterization window.

Operating Modes

To maximize utilization of the memory at each clock edge, the Virtex-II block SelectRAM-II memory supports three different write modes. The Read-Before-Write mode offers the flexibility of using the data output bus during a write operation on the same port. Output latch values are determined by the configuration. This choice increases the effective bandwidth of the Block Memory.

Note that the Virtex SelecRAM+ supports only the Write First mode.

Read Operation

Read operations are synchronous to the rising edge of the clock. The data in the memory location selected by the address appears on the DOUT port after the rising edge of the clock.

Write Operation

Write operations are synchronous to the rising edge of the clock. The data on the DIN port is written into the memory location selected by the address on the rising edge of the clock when WE is active. The user can configure the memory in one of the three ways described below to determine the behavior of the DOUT port during a write cycle. Note that the timing diagram and description of the write modes below assume that the memory has been configured without input registering and additional output registers.

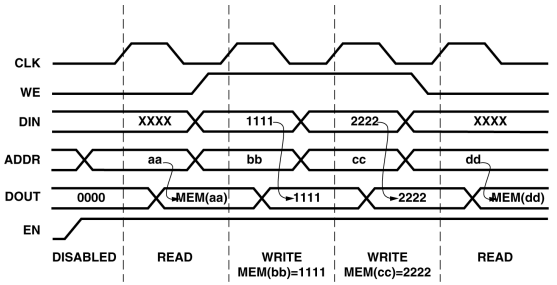

Figure 5: Write First Mode Waveform

Write First or Read-After-Write (or Transparent) Mode

In write first mode, data input is loaded simultaneously with a write operation on the DOUT port. As shown in Figure 5, the data input is stored in memory and mirrored on the output.

Read First or Read-Before-Write Mode

In this mode, data previously stored at the write address appears on the output latches. Data input is stored in memory and the prior content of that location driven on the output, during the same clock cycle (shown in Figure 6).

No Change or No-Read-On-Write Mode

In No Change mode, the DOUT port remains unchanged during a write operation. As shown in Figure 7, data output is still the last read data and is unaffected by a write operation on the same port.

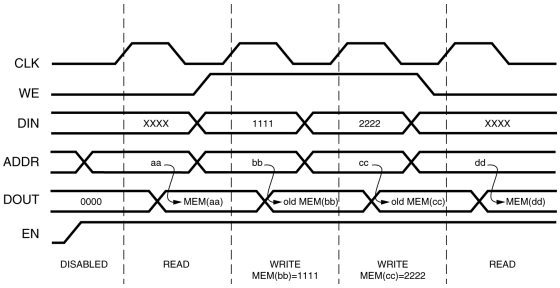

Figure 6: Read First Mode Waveform

```
MEMORY_INITIALIZATION_RADIX=16;
MEMORY_INITIALIZATION_VECTOR=123, 456,
aaaa;
```

Figure 8: An example of a *coe* file for a Virtex-II Single-Port Block RAM.

Mode configuration is static. One of these three modes is set individually for each port by an attribute. The default mode is write first.

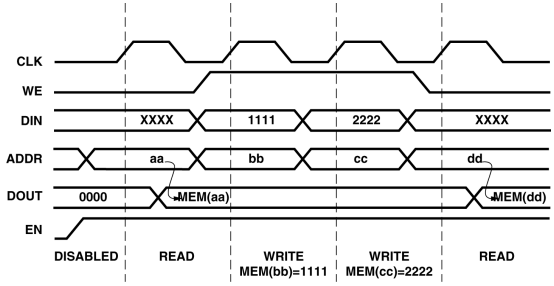

Figure 7: No Change on Write Mode Waveform

Specifying Memory Contents

The initial contents of the memory can be assigned by specifying the desired information in a separate text file

called a *coe* file. To select and load a *coe* file, press the "Load Init Values..." button on the parameterization window and choose the desired file from the from dialog box. An example of a *coe* file for a 3 by 16 RAM is shown in Figure 8.

When specifying the initial contents for a memory in a *coe* file, the keywords MEMORY_INITIALIZATION_RADIX and MEMORY_INITIALIZATION_VECTOR can be used. The MEMORY_INITIALIZATION_VECTOR takes the form of a sequence of comma-separated values, one value per memory location, terminated by a semicolon. Any amount of white space, including new lines, can be included in the vector to enhance readability. The format of an individual

value in the vector will depend on the MEMORY_INITIALIZATION_RADIX value, which can be 2, 10, or 16 (the default value is 16). The vector must be consistent with the MEMORY_INITIALIZATION_RADIX value and must fall within the range of 0 to 2^{DATA_WIDTH} -1. Values must not be negative.

Core Resource Utilization

The number of Block RAM primitives required depends on the values of data depth and width fields selected in the CORE Generator parameterization window. This value must be at least (depth_width)/18432 and will exceed this number for many configurations.

For some memory depths, extra logic is required to decode the address and multiplex the outputs from various primitives. Virtex or Virtex-II CLB slices are used to provide this functionality. The number of slices required depends on the way that the depth is constructed from the primitives, the data width, and the implementation of any decoding or multiplexing.

For more information about the number of block RAMs in each device, please refer to Tables 4 through 6.

Table 2: Parameter File information for Virtex-II

Parameter Name	Type	Notes
Component Name	String	Up to 256 characters
Width	Integer	Ranges from 1 to 256
Depth	Integer	Ranges from 2 to 1M.
Port Configuration	String	Default=read and write Options are: read and write read only
Write Mode	String	Default=read after write, Options are: read after write read before write no read on write
Load Init File	Boolean	Default=false false=Use Global Init Value Only true=Use loaded *coe* file
Global Init Value	String	Default=0
Coefficient File	String	Default=null
Enable Pin	Boolean	Default=false
Handshaking Pins: ND, RDY, RFD	Boolean	Default=false
Register Inputs	Boolean	Default=false
Additional Output Pipe Stages	Integer	Default=0 0=No additional output registers
Init Pin	Boolean	Default=false
Init Value	Integer	Default=0

Table 2: Parameter File information for Virtex-II

Parameter Name	Type	Notes
Has Limit Data Pitch	Boolean	Default=false
Limit Data Pitch	Integer	Default=18 Options are: 18 and 36

Table 3: Parameter File information for Virtex

Parameter Name	Type	Notes
Component Name	String	Up to 256 characters
Width	Integer	Ranges from 1 to 256
Depth	Integer	Ranges from 2 to 256K
Port Configuration	String	Default=read and write Options are: read and write read only
Write Mode	String	Default=read after write
Global Init Value	String	Default="0"
Load Init File	Boolean	Default=false false=Use Global Init Value Only true=Use loaded COE file
Coefficient File	String	Default=null
Enable Pin	Boolean	Default=false
Handshaking Pins: ND, RDY, RFD	Boolean	Default=false
Register Inputs	Boolean	Default=false
Additional Output Pipe Stages	Integer	Default=0 0=No additional output registers
Init Pin	Boolean	Default=false
Init Value	Integer	Default=0 (cannot be altered)
Has Limit Data Pitch	Boolean	Default=false
Limit Data Pitch	Integer	Default=8 Options are: 8 and 16

Table 4: Virtex Device Block RAM Counts

Devices	# Blocks	Total Block (bits)
xcv50	8	32,768
xcv100	10	40,910
xcv150	12	49,152
xcv200	14	57,344
xcv300	16	65,536
xcv400	20	81,920
xcv600	24	98,304
xcv800	28	114,688
xcv1000	32	131,072

Table 5: Virtex-E Device Block RAM Counts

Devices	# Blocks	Total Block (bits)
xcv50E	16	65,536
xcv100E	20	81,920
xcv200E	28	114,688
xcv300R	32	131,072
xcv400E	40	163,840
xcv600E	72	294,912
xcv1000E	96	393,216
xcv1600E	144	589,824
xcv2000E	160	655,360
xcv2600E	184	753,664
xcv3200E	208	851,968
xcv405E	140	573,440
xcv812E	280	1,146,880

Table 6: Virtex-II Device Block RAM Counts

Devices	# Blocks	Total Block (Kb)
xc2v250	24	432
xc2v500	32	576
xc2v1000	40	720
xc2v1500	48	864
xc2v2000	56	1,008
xc2v3000	96	1,728
xc2v4000	120	2,160
xc2v6000	144	2,592
xc2v8000	168	3,026
xc2v10000	192	3,456

Ordering Information

This core can be downloaded free of charge from the Xilinx IP Center (http://www.xilinx.com/ipcenter) for use with the Xilinx CORE Generator System V3.1i and later. The CORE Generator System tool is bundled with all Xilinx Alliance and Foundation Series Software packages.

To order online, visit the Xilinx Silicon Expresso Cafe at http://toolbox.xilinx.com/cgi-bin/xilinx.storefront/241669816/catalog//1006).

Xilinx software can also be ordered through your local Xilinx sales office. Information on the sales office nearest you is available at http://www.xilinx.com/company/sales.htm.