Single Port Block Memory for Virtex™-II V2.0

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Xilinx Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com/ipcenter
Support: support.xilinx.com

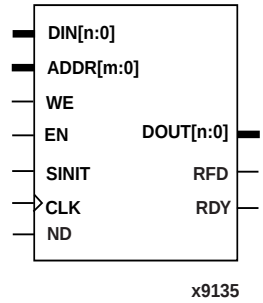

Figure 1: Core Schematic Symbol

Features

- Fully synchronous drop-in modules for Virtex™-II families; uses Virtex™-II block memory for performance and efficiency
- Supports all three Virtex™-II write mode options: read after write, read before write; no read on write
- Supports RAM functions
- Supports data widths from 1 to 256 bits; and memory depths from 512 to 1M words
- Available in the Xilinx CORE Generator™ System V3.1i

Functional Description

The Block Memory module is generated based on the user specified width and depth. This module is composed of single or multiply Virtex™-II RAM Blocks depending on the configuration.

During a write operation the data value is stored at the location selected by the address. The Block Memory's data input and address widths are configured by the user. Three different "write mode" options determine the behavior of the data output port (read port) when a write operation occurs. The three options are (1) read after write, (2) read before write and (3) no change on write.

When the Block Memory is enabled, all memory operations occur on the rising edge of the clock input (CLK). When the Block Memory is disabled (enable inactive), the memory configuration and output value remain unaltered.

During a read operation the memory contents at the location selected by the address will appear at the module's output. When synchronous initialization (SINIT) is active, the module's outputs are synchronously reset to a user defined value. SINIT does not affect the contents of the memory or write operations.

For additional information on Virtex™-II Block Memory features, please refer to the *Virtex™-II Handbook*.

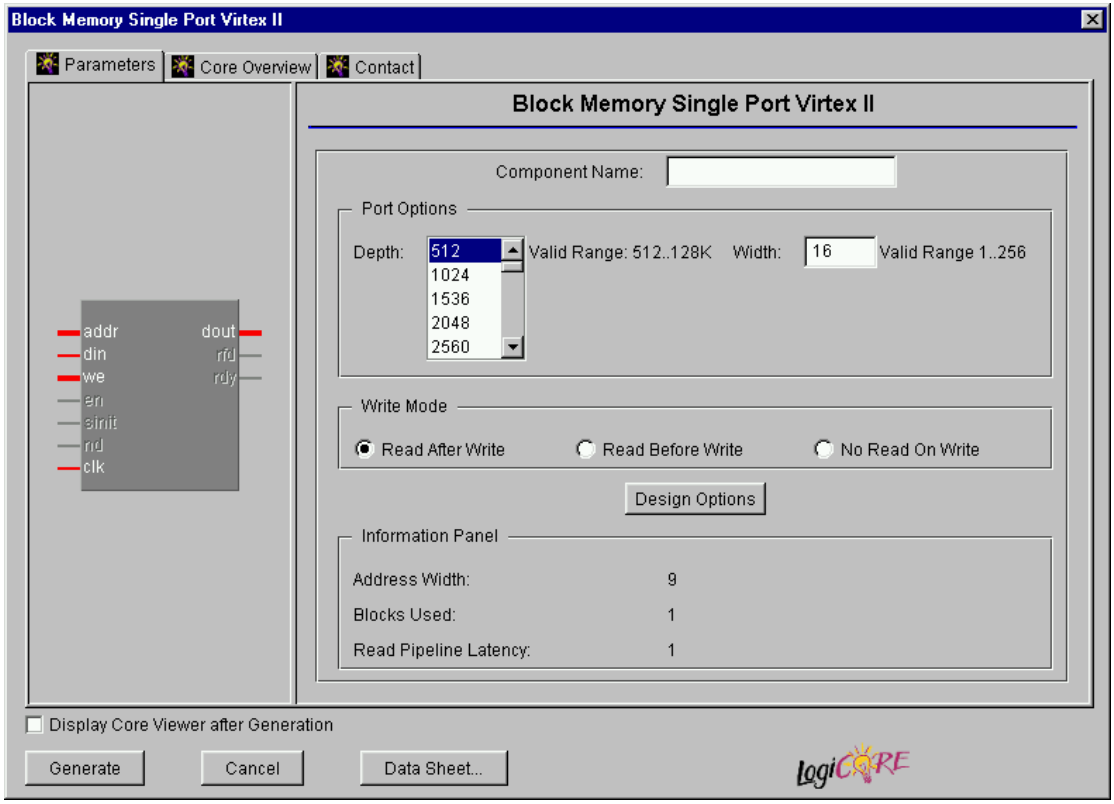

Figure 2: Single Port Block Memory Main Parameterization Window

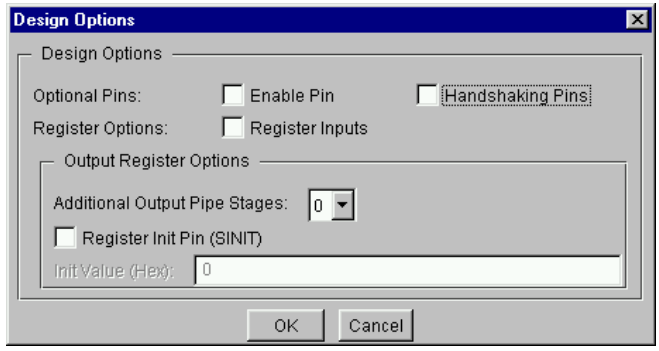

Figure 3: Single Port Design Options Window

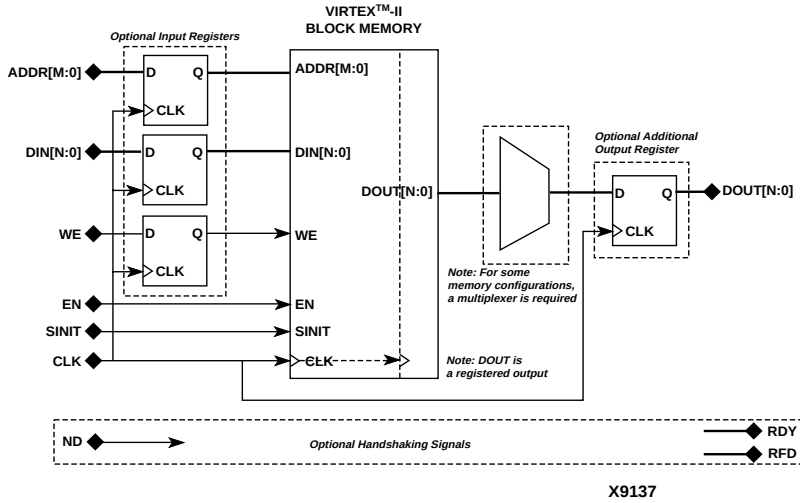

Figure 4: Single Port Memory Block Diagram

Table 1: Core Signal Pinout

Signal	Direction	Description
DIN[n:0]	Input	**Data Input**: data written into memory.
ADDR [m:0]	Input	**Address**: memory location for data written to/read from.
WE (Optional)	Input	**Write Enable**: allows data transfer input into memory. (Active High)
EN (Optional)	Input	**Enable**: enables access to memory via read and write operations. (Active High)
SINIT (Optional)	Input	**Synchronous Initialization**: forces module outputs to predefined state.
CLK	Input	**Clock**: all memory operations synchronous with rising edge of clock input. When memory is enabled, all control signals, input/output data are registered on the rising edge of clock.
ND (Optional)	Input	**New Data**: indicates new and valid address on ADDR.(Active High)
DOUT[n:0]	Output	**Data Output**: synchronous output of the memory.
RFD (Optional)	Output	**Ready for Data**: indicates that memory is ready for new address. (Active High)
RDY (Optional)	Output	**Ready for Data**: indicates valid data on DOUT port. (Active High)

Pinout

Port names for the core module are shown in Figure 1 and described in Table 1. The inclusion of some ports on the module is optional; exclusion of these ports will alter the function of the module. The optional ports are marked in Table 1. For additional information on Virtex-II Block RAM refer to the *Virtex-II Handbook*.

Clock - CLK

Block Memory is fully synchronous with clock input. All input pins have setup time referenced to the port CLK pin. The DOUT port has a clock-to-out time referenced to the CLK pin.

Enable - EN

The enable pin affects the read, write, and SINIT functionality of the port. When the Block Memory has an inactive enable pin, the output pins are held in the previous state and writing to the memory is disabled.

Write Enable - WE

Activating the write enable pin enables memory locations to be written. When active, the contents of the DIN bus is written to memory at the address pointed to by the ADDR bus. The output latches are loaded or not loaded according to the write configuration (Write First, Read First, No Change). When WE is inactive, a read operation occurs, and the contents of the memory addressed by the ADDR bus are driven on the DOUT bus.

Synchronous Initialization - SINIT

The SINIT pin forces the data output latches to contain the predefined SINIT value. The data output ports are synchronously asserted to the user-defined SINIT value. This operation does not affect memory locations and does not disturb write operations. Like the read and write operation, the SINIT function is active only when the enable pin of the port is active.

Address Bus - ADDR[m:0]

The address bus which selects the memory location for read or write access.

Data In Bus - DIN[n:0]

DIN bus provides the data value to be written into the memory. Data input and output signals are always busses; that is, in a 1-bit width configuration, the data input signal is DIN[0] and the data output signal is DOUT[0].

Data Out Bus - DOUT[n:0]

DOUT bus reflects the contents of memory locations referenced by the address bus during a read operation. During a write operation, in the Write First or Read First Configuration, the data-out bus reflects either the DIN bus or the previous stored value before write. During a write operation in no change mode, the data-out bus is not affected.

New Data - ND

Indicates that there is a new and valid address on ADDR Port.

Ready for Data - RFD

Indicates that the memory is ready to accept a new address. RFD is always true except when EN is inactive.

Output Ready (Valid) - RDY

Indicates valid ouput on DOUT port. RDY will lag ND by the latency of the block memory.

CORE Generator Parameters

The CORE Generator parameterization window for this module is shown in Figure 2 and Figure 3. In Figure 2, the window allows the memory ports to be defined. An information window, which is useful in verifying that the total number of blocks required does not exceed those available on the targeted device, is also shown at the bottom. In Figure 3, the window allows configuration of the design options. The available options are described below.

Definition of GUI Interface Fields

- **Component Name**: Enter a name for the output files generated for this module (up to 256 characters).
- **Port Options**:
  - **Depth**: Enter the number of words in the memory. The range of values is 512 to 1,048,576 (1M). Entries not divisible by 512 will be rounded up to the next highest multiple of 512. The absolute maximum number of words is 1M. Cores should not exceed the number of Block RAM primitives available in the targeted device.
  - **Width**: Select the data bit width. The width values can be between 1 and 256. Cores should not exceed the number of Block RAM primitives available in the targeted device.
- **Write Mode**: Select one; the default is “read after write.”
  - **Read after Write**: On the same clock edge that writes the input data into memory, the input data is transferred onto the DOUT port.
  - **Read before Write**: On the same clock edge that writes the input data into memory, the current data in the addressed memory location is transferred onto the DOUT port.
  - **No Read on Write**: A write operation has no effect on the content of the DOUT port. The DOUT port is updated when WE is inactive.
- **Design Option**: Press this button to display the design options dialogue box on the screen. The resulting display is shown in Figure 3.
- **Information Panel**: Window provides feedback on the memory based on the selected parameter values.
  - **Address Width**: Shows the number of bits needed to address all of the words in the memory.
  - **Blocks Used**: Shows the number of Block RAM primitives required to implement the specified Memory Depth and Width.
  - **Read Pipeline Latency**: Calculates the latency from the Address port (ADDR) to the data output port (DOUT).
- **Generate**: Select to generate the block memory module. Make sure that the parameters are correctly selected for the particular application before executing this option.
- **Cancel:** Select to close window and return to the Core Generator.
- **Datasheet:** Select to generate a PDF version of this document.

Design Options

- **Optional Pins**:
  - **Enable Pin**: Check the box to include the enable port on the module; uncheck the box to remove it. This port provides an enable for all memory read and write operations. When it is inactive, the memory is disabled.
  - **Handshaking Pins**: Check the box to include the following ports; uncheck the box to remove them.
    - **ND** [New Data]: Signals a new and valid memory address whenever active. This port has no effect

on the memory read and write operations. ND is only valid when RFD is active.
  - **RFD** [Ready For Data]: Indicates that the memory can accept new addresses. Always active when the memory is enabled.
  - **RDY** [Output is Ready]: Indicates to the user that the data on the output is valid. RDY will lag ND by the latency of the module.
- **Register Options**:
  - **Register Inputs**: Check this box to register ports DIN, ADDR, and WE prior to accessing block memory. See Figure 4.
- **Output Register Options**:
  - **Additional Output Pipe Stages**: Select "1" to enable an additional register on the output of the memory; select "0" to disable an additional register on the output of the memory. See Figure 4.
  - **Init pin**: Check box to add the synchronous port SINIT to the memory. When this signal is active, the output of the memory is set to a pre-defined value. Enabling this port has no affect on the contents of the memory.
    - **Init value** (HEX value): Enter the HEX value that the output port will get set to when the SINIT port is true.
- **Close**: Select to close window and return to main parameterization window.

Operating Modes

To maximize utilization of the True Dual-Port memory at each clock edge, the block SelectRAM-II memory supports three different write modes. Each port's write mode is independently configurable. The "read before write" mode offers the flexibility of using the data output bus during a write operation on the same port. Output latch values are determined by the configuration. This choice increases the effective bandwidth of the Block Memory.

Read Operation

Read operations are synchronous to the rising edge of the clock. The data in the memory location selected by the address apears on the DOUT port after the rising edge of the clock.

Write Operation

Write operations are synchronous to the rising edge of the clock. The data on the DIN port is written into the memory location selected by the address on the rising edge of the clock when WE is active. The user can configure the memory in one of three ways to determine the behavior of the DOUT port during a write cycle. Each port's write mode is independently configurable. Note that the timing diagram and description of the write modes below assume that the memory has been configured without input registering and additional output registers.

Write First (or Transparent) Mode

In write first mode, data input is loaded simultaneously with a write operation on the DOUT port. As shown in Figure 5, the data input is stored in memory and mirrored on the output.

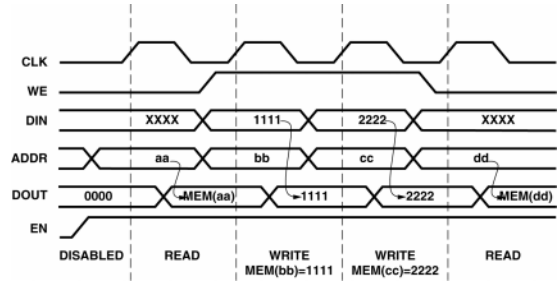

Figure 5: Write First Mode Waveform

Read First or Read-Before-Write Mode

In this mode, data previously stored at the write address appears on the output latches. Data input is stored in memory and prior contents of that location is driven on the output, during the same clock cycle (shown in Figure 6).

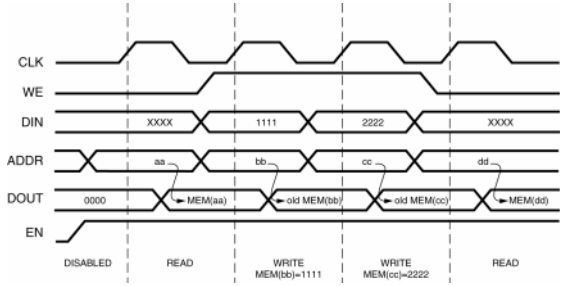

Figure 6: Read First Mode Waveform

No Change Mode

In no change mode, the DOUT port remain unchanged during a write operation. As shown in Figure 7, data output is still the last read data and is unaffected by a write operation on the same port. Mode configuration is static. One of these three modes is set individually for each port by an attribute. The default mode is write first.

Conflict Resolution

Virtex-II block memory is True Single-Port RAM that allows both ports to simultaneously access the same memory location. When one port writes to a given memory location, the other port must not address that memory locationl (for a write/read) within the clock-to-clock setup window. Conflicts do not cause any physical damage to BlockRAM cells. For

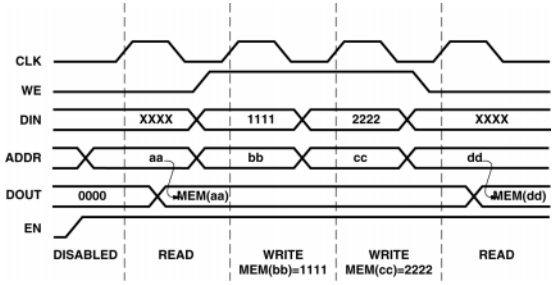

Figure 7: No Change on Write Mode Waveform

more information on conflict resolution, refer to the *Virtex™-II Handbook*.

Core Resource Utilization

The number of Block RAM primitives required is dependent on the values of data depth and width fields selected in the CORE Generator parameterization window, and is atleast (depth_width)/18432 and will exceed this number for many configurations.

For some memory depths extra logic is required to decode the address and multiplex the outputs from various primitives. Virtex™-II CLB slices are used to provide this functionality. The number of slices required depends on the way that the depth is constructed from the primitives, the data width, and the implementation of any decoding or multiplexing.

Table 2: Parameter File Information

Parameter Name	Type	Notes
Component Name	String	Up to 256 characters
Width	Integer	Ranges from 1 to 256
Depth	Integer	Ranges from 512 to 1Meg with increments of 512
Write Modes	String	Default=read after write, Options are: read after write read before write no read on write
Enable	Boolean	Default=false
Handshaking Pins: ND, RDY, RFD	Boolean	Default=false
Register Inputs	Boolean	Default=false
Additional Output Pipe Stages	Integer	Default=0 0=”No additional output registers”
Synchronous Initialization	Boolean	Default=false
Synchronous Initialization	Integer	Default=”0”

Ordering Information

This core may be downloaded free of cost from the Xilinx IP Center (http://www.xilinx.com/ipcenter) for use with the Xilinx CORE Generator™ System V3.1i and later. The CORE Generator System tool is bundled with all Xilinx Alliance and Foundation Series Software packages.

To order online, visit the Xilinx Silicon Expresso Cafe at http://toolbox.xilinx.com/cgi-bin/xilinx.storefront/241669816/catalog//1006).

Xilinx software may also be ordered through your local Xilinx sales office. Information on the sales office nearest you is available at http://www.xilinx.com/company/sales.htm.