Dynamic Constant Coefficient Multiplier V2.0

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Features

- Combinatorial design with optional pipelined construction for increased throughput
- Multiplies a variable **A** times a constant **B**
  - The **A** value can range from 4 to 32 bits
  - The **B** value can range from 4 to 26 bits
- Independent **A** and **B** word size
- Hardware selection of signed or unsigned input data
- Full precision output
- Supports 2's complement signed and unsigned magnitude coefficient
- Drop-in modules for Virtex, Virtex™-E, Spartan™-II, and Virtex™-II FPGAs.
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator™ System V3.1i.

Functional Description

This parameterized module multiplies an N-bit variable times an M-bit constant and produces an N+M bit result. Internal coefficient multiplication tables are stored in distributed RAM-based look-up tables (LUTs), taking advantage of the FPGA look-up table architecture to deliver an efficient, high speed, parallel implementation.

The Dynamic Constant Coefficient Multiplier (DKCM) is used where the value of an incoming variable needs to be multiplied by a number that does not change, or which changes only infrequently. This is often the case in scaling functions, FIR filters, IIR filters, etc. The variable and constant bit widths can be set independently, allowing the user to multiply values with different bit widths. The module automatically adjusts the signed and unsigned data to properly handle differences in bit width.

The variable and constant can be independently selected to be 2's complement signed or unsigned magnitude-only values. The module will automatically handle a signed multiplied by an unsigned number, two signed numbers, or two unsigned numbers.

The sign of the input data is selected by the state of the module's SIGNEDA input pin. This pin may be tied high or low, or may be used to enable cascading of multiple Dynamic Constant Coefficient Multipliers (DKCM) to form larger multipliers.

The module allows the constant **B** to be changed by providing the circuitry to recalculate the contents of internal multiplication tables. Since the tables are 16-words deep, 16 clock cycles are required to modify the constant. The process of updating the constant is initiated by providing the new constant on the DATAB input and asserting the LOADB input. The BUSY output will go high for 16 clock cycles, indicating that internal tables are being updated and that the multiplier's output is undefined. This process is illustrated in Figure 3.

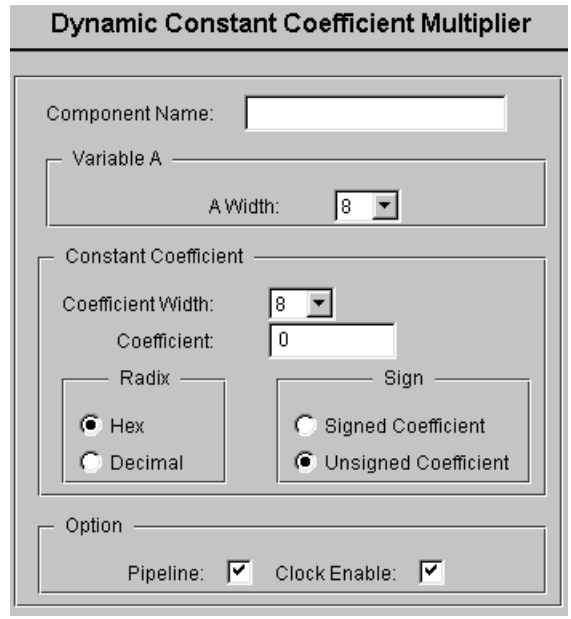

Figure 1: Parameterization Window

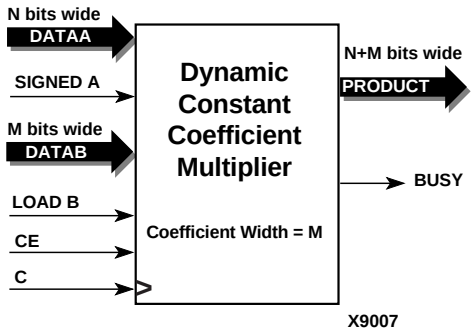

Figure 2: Schematic Symbol

Pinout

Port names for the schematic symbol are shown in Figure 2 and described in Table 1.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 1. The parameters are as follows:

- **Component Name**: Enter a name for the component.
- **A Width**: Select an input bit width from the pull-down menu for the variable width. The valid range is 4 to 32.
- **Coefficient Width**: Select an input bit width from the pull-down menu for the constant width. The valid range is 4 to 26.
- **Coefficient**: Enter the value of the desired constant.
- **Signed Coefficient**: Set the sign of the constant to Signed or Unsigned.
- **Radix**: Hexadecimal or Decimal representation of the constant.
- **Pipeline:** Choose whether the multiplier should be pipelined or purely combinatorial (has no effect on constant-reload logic which always contains registers).
- **Clock Enable:** If pipelined construction is chosen for the multiplier, a clock-enable may also be selected. This active high input freezes the partial results in the pipeline when taken low, and normal operation resumes when the pin returns high (has no effect on the constant-reload logic).

Multiplier Latency

The total latency (number of clocks required to get the first output) is a function of the width of variable **A**. Table 2 shows the latency for the possible bit widths of **A**.

The module can be constructed in a pipelined or combinatorial fashion. In combinatorial mode, the PRODUCT output is a combinatorial function of DATAA and SIGNEDA inputs, and the contents of the internal look-up tables: Latency = 0.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
DATAA[n:0]	Input	Parallel data input, N-bits wide
SIGNEDA	Input	Indicates the sign/unsigned status of the data being applied to the DATAA input. High=signed, Low=unsigned.
DATAB[m:0]	Input	Constant data input, M-bits wide
LOADB	Input	Assert to reload internal coefficient with value presented on DATAB input.
CE	Input	Clock Enable, active high. This is an optional pin that may only be selected when pipelined-mode is chosen. Affects only the multiplier pipeline's operation. (i.e. has no impact on logic that reloads the coefficient)
C	Input	CLOCK – with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
PROD[m+n+1]	Output	Parallel Data Out, N+M bits wide.
BUSY	Output	When high, indicates that the DKCM is in the process of modifying its internal multiplication look-up tables. Values on DATAA, SIGNEDA, and CE are ignored until BUSY returns low.

Table 2: Multiplier Latency

Data A Bit Width	Latency (# Clocks)
4 to 8	2
9 to 16	3
17 to 32	4

Ordering Information

This macro comes free with the Xilinx CORE Generator™ System. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

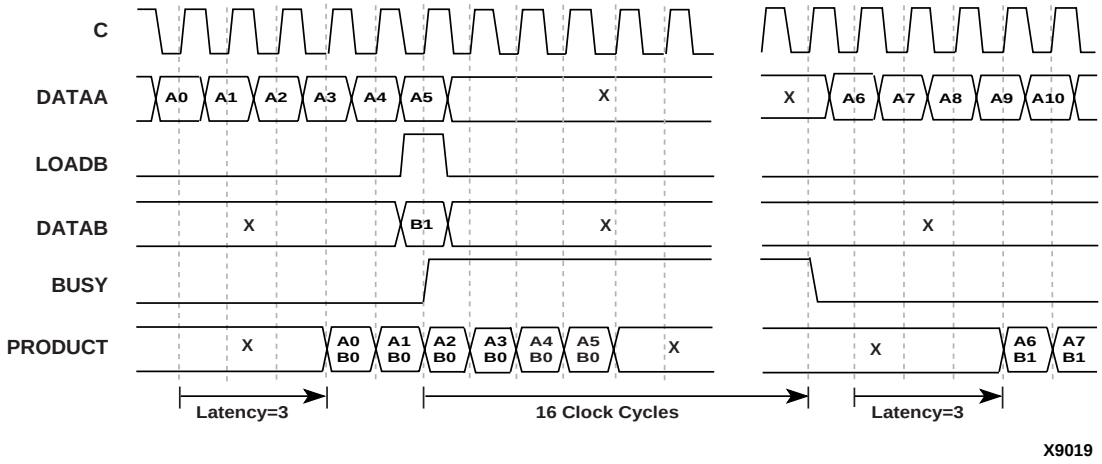

Figure 3: Timing Diagram Showing Procedure For Reloading Coefficient