T1 Deframer

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Features

- Supports T1-D4 and T1-ESF frame structures
- Fully compliant with CCITT G.704 (G.706, G.733)
- T1-D4 recovers 12-frame multiframe
- T1-ESF recovers 24-frame multiframe
- Provides support for recovering & inserting robbed bit signalling
- Provides support for recovering and generating CRC6
- Provides support for recovering and inserting serial data link (ESF only)
- Full detection of yellow alarm condition
- FAW bit error monitoring allows BER estimation
- Fast frame alignment time
- Fully synchronous design

Applications

- ISDN Primary Rate Access
- Multiplexing equipment
- Satellite communications
- Digital PABX
- High speed computer links

General Description

The device implements the basic timing extraction block used in T1 applications. The block accepts a T1 (ESF or D4) bearer on its input, synchronizes to it, and generates various common bit and timeslot location and control signals as follows:

- Frame Alignment Location
- Data Location
- Multiframe synchronization
- FAW Location
- A Bit Location (ESF only)
- CRC Bit Location (ESF only)
- CRC Done Location (ESF only)
- M Bit Location (ESF only)
- S Bit Location (D4 only)
- F Bit Location
- FAW Error Count
- Synchronization Loss indicator
- Back Alarm Indicator

Delayed versions of some signals are generated to allow efficient connections to blocks further down stream. These delayed output signals can be configured to occur an integer number of data bit cycles after the main signals, as set by the Output_Delay input.

LogiCORE™ Facts

Core Specifics	
Device Family	Virtex™, Virtex™-E, Spartan™ II
Slices Used	268
IOBs Used	139
CLKIOBs Used	1
System Clock fmax	>40MHz
Device Features Used	-
Provided with Core	
Documentation	Product Specification
Design File Formats	Targeted EDIF
Constraint Files	.ucf file
Verification Tool	ModelSim v5.4 Demonstration VHDL and Verilog test benches supplied
Schematic Symbols	-
Evaluation Model	Post-layout .vhd, .veri
Reference designs & application notes	-
Additional Items	-
Design Tool Requirements	
Xilinx Core Tools	Design Manager 3.2
Entry/Verification Tool	FPGA Express 3.4 ModelSim v5.4
Support	
Support provided by Xilinx	

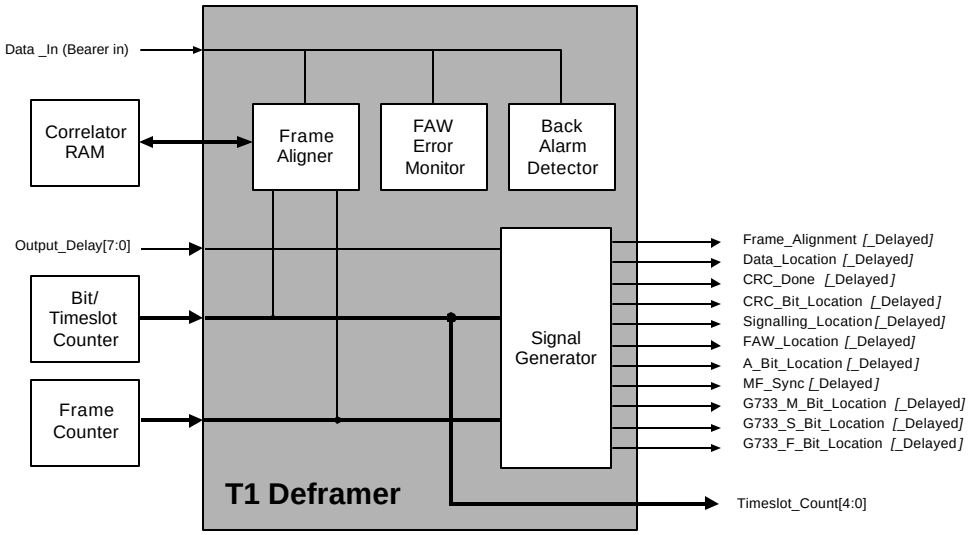


Figure 1: Block Diagram

Functional Description

Synchronizer

This state machine handles the acquisition and loss of frame alignment. Its state transitions are as shown in adjacent figure.

The machine produces two outputs, a Sync_Loss signal, which indicates when the frame lock has been found, and a Global_Counter_Synchronisation signal, which indicates when the counters are to be reloaded to synchronize them to the multiframe.

Signal Generator

This block generates all the timing and location signals required by external modules. Delayed versions of many of the signals are provided to allow efficient system design. The delay values of these signals is readily programmable by means of the Output_Delay input.

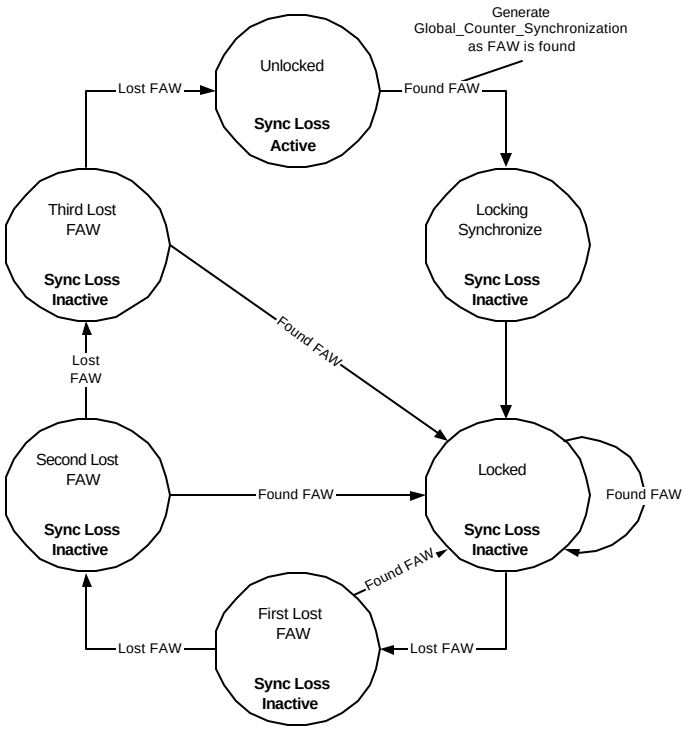


Figure 2: Synchronizer State Machine

FAW Error Checker

This block examines the bits of the FAW acquired over the last complete multiframe, and compares them with the expected values. The number of bit errors is calculated, and presented as a number on the FAW_Error_ Count[3:0] signal. In ESF mode, there will be between 0 and 6 errors per FAW. In D4 mode, there will be between 0 and 11 errors: the last FAW bit is not tested as it indicates a Back Alarm condition. The FAW_Error_Count[3:0] signal becomes valid on the Frame_Alignment signal, and should be latched by the rising edge of this signal.

ESF Back Alarm

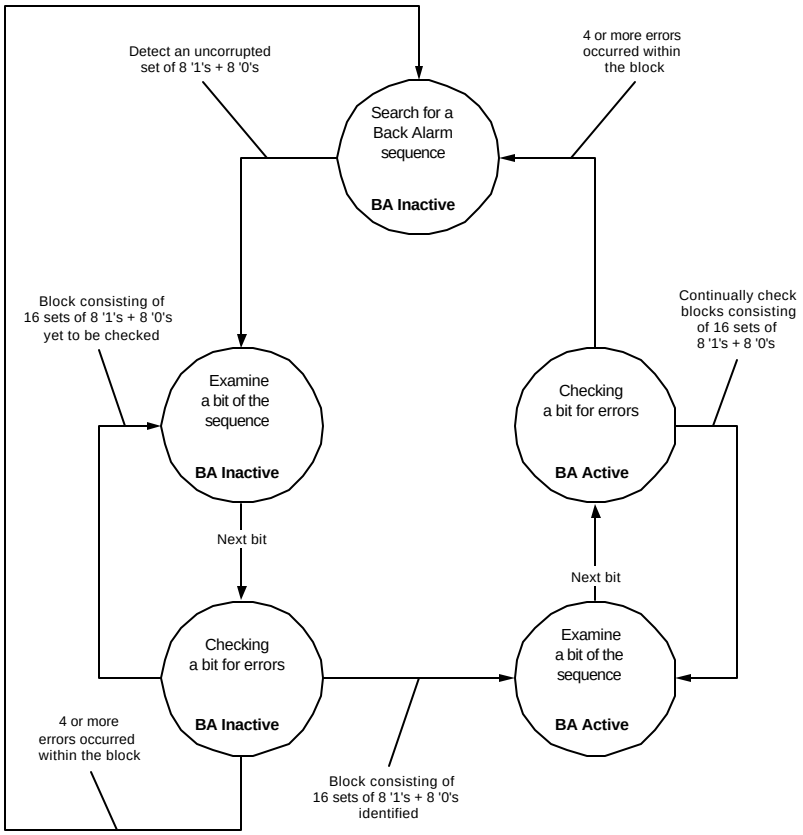
The status of the ESF Back Alarm is carried by the data link message bits (M bits). These message bits are actually the F bits of every other frame, starting with the first frame of the 24-frame ESF multiframe. Thus the overall rate of the data link is 4Kbps. The Back Alarm is indicated by transmitting a sequence of eight '1's and eight '0's (1111111100000000) down this data link and can be used to indicate the Loss of Frame Alignment (LFA) condition.

The T1 Deframer automatically detects this sequence on an incoming bearer and activates the Back_Alarm signal. The detection process has been optimized to correctly detect a back alarm condition, even in the presence of a high bit error rate on the incoming bearer. The sequence followed in the ESF Back Alarm detection process is as outlined in the figure below.

D4 Back Alarm

The status of the D4 Back Alarm is carried by the F-bit in the last frame of a 12-frame T1 D4 multiframe. The Back Alarm condition is indicated by changing this bit from a '0' to a '1'. The T1 Deframer automatically detects this change on an incoming bearer and activates the Back_Alarm signal. The detection process has been optimized to correctly detect a back alarm condition even in the presence of a high bit error rate on the incoming bearer. This is done by checking the most recently detected Back Alarm bit in conjunction with the previous three most recently received Back Alarm bits. The Back Alarm is set to active if any three out of these four bits is '1' and is set to inactive if two or more of these bits if '0'.

Figure 3: ESF Back Alarm Method



RAM Interface

The RAM Interface is designed for use with a synchronous RAM such as the Xilinx Select or Block RAM (256 x 28 bits). The RAM read / modify / write cycle takes six system clock cycles. The cycle is initiated each time a Data_In_Valid pulse occurs. The data addressed is expected to be valid two clock cycles later. The RAM data, CorrelatorDI, is registered inside the core when both CorrelatorME and CorrelatorMA are active during the read cycle (CorrelatorRNW high). Three clock cycles later, the modified data (CorrelatorDI) should be written to the RAM on the rising edge of the system clock when both CorrelatorME and CorrelatorMA are high and Correlator-RNW is low.

Bearer Data Synchronization

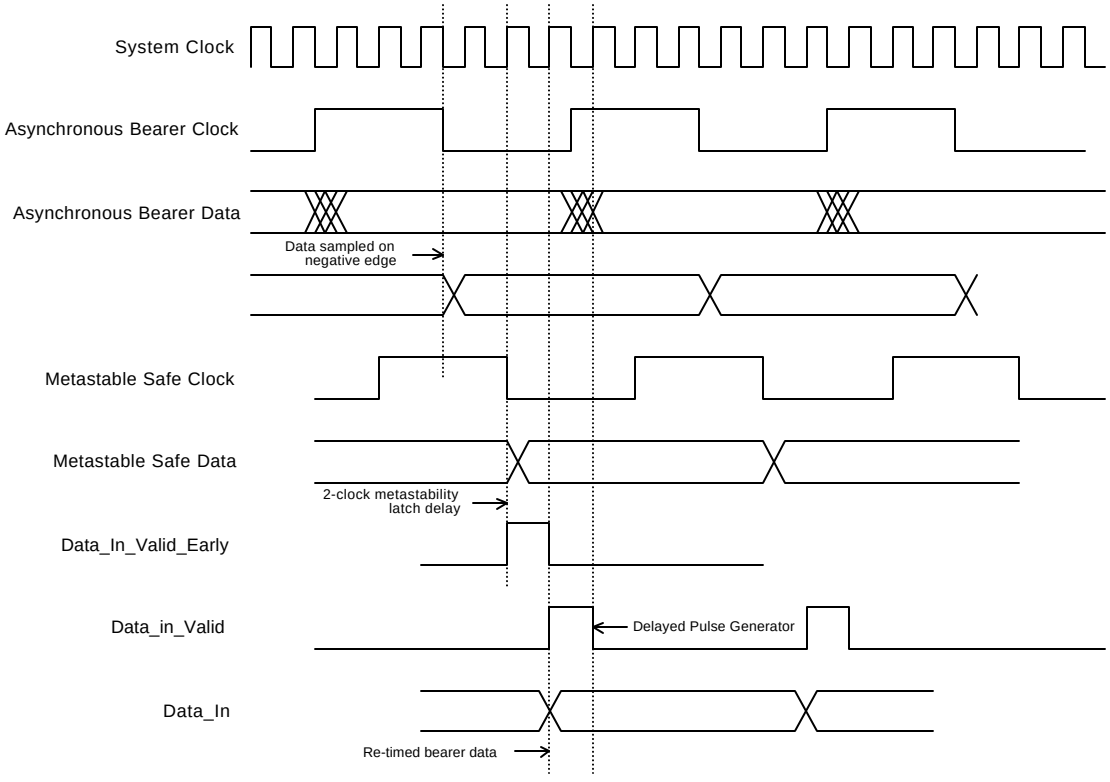
As the Deframer is a fully synchronous design, it requires synchronous inputs in order to function correctly. If the bearer data, and bearer clock are not synchronized to the system clock, a data synchronizer will be required to re-time these signals and to eliminate metastability problems.

The data synchronizer supplied with the Deframer uses a pulse generator to produce the single-clock-width Data_Valid signal required by the Deframer. The Bearer data is sampled two system clock pulses into its period to ensure maximum stability. Then it is re-timed to coincide with the Data_Valid signal and to provide a stable setup and hold period.

Two metastability latches are provided on both the data and clock inputs to eliminate metastability problems (as shown in the diagram below).

Due to the re-sampling of the Bearer Clock by the System Clock, there will be some jitter introduced into the period of the Bearer Data. As the System Clock is at least six times the bearer clock, this jitter will be quite small.

Figure 4: Synchronizer Timings



Pinout

Please Note: (i) All ports are active high (positive) logic unless specifically stated otherwise.

(ii) The numbering scheme represents the value of the Frame_Bit_Count(7:0) and the Multiframe_Count(4:0) signals and thus differs from the CCITT system..

Signal	Direction	Description
SYSTEM		
Clock	I	System Clock.
A_Reset	I	Asynchronous Reset (Active Low).
S_Reset	I	Synchronous Reset (Active Low).
Data_In	I	Data processed by the T1 Deframer.
Data_In_Valid	I	Valid data bit location signal.
Data_In_Valid_Early	I	Version of Data_In_Valid signal that preceeds it by 1 System Clock cycle.
CONTROL		
R_G733_D4_MFAS_Present	I	Register bit indicating whether multiframe is present.
R_G733_T1ESF_D4_Mode	I	Register bit used to set G.733 T1-D4 mode.
R_G733_Enable	I	Register bit that enabled the G,733 Frame Aligner.
Output_Delay[7:0]	I	Required output delay as an integer number of data bit cycles. Limited to 192.
COUNTERS		
Frame_Count[4:0]	I	Frame number within the current multiframe. This count changes at the frame rate. It counts between 0 - 23 for T1 ESF systems and 0 - 11 for T1 D4 Frame systems
Frame_Count_Enable	O	When high, causes the Frame counter to count.
Frame_Count_Load	O	When high, requests the Frame counter to perform a parallel load of the Frame_Count_Load_Value.
Frame_Count_Load_Value[4:0]	O	Sets the value loaded when Frame_Count_Load is taken high.
Bit_Count[7:0]	I	Bit number within the current frame. It counts between 0 and 192. The Frame Bit occurs at bit count 192. (Note: Differs from G.704 definition.)
Bit_Count_Enable	O	When high, causes the Bit counter to count.
Bit_Count_Load	O	When high, requests the Bit counter to perform a parallel load of the Bit_Count_Load_Value.
Bit_Count_Load_Value	O	Sets the value loaded when Bit_Count_Load is taken high.
Timeslot_Count[4:0]	O	Timeslot number within the current frame. It is basically the top 5 bits of the bit count.
CORRELATOR RAM SIGNALS		
CorrelatorDO[27:0]	I	Data input from external correlator RAM.
CorrelatorDI[27:0]	O	Data output to external correlator RAM.
CorrelatorRNW	O	Correlator Read Not Write.
CorrelatorME	O	Correlator Memory Enable.
CorrelatorMA	O	Correlator Memor Access.
BIT, WORD & FRAME SIGNALS Note: The T1 Deframer also produces delayed versions of these signals that are delayed by an integer number of data bit cycles, set through the Output_Delay input. Note that this delay must less than 1 frame (i.e. 192 max.)		
Frame_Alignment	O	Frame Alignment signal showing start of multiframe alignment.
Data_Location	O	Data Location signal.
CRC_Done	O	CRC Frame Complete signal (T1-ESF only).
CRC_Bit_Location	O	Signal indicating location of CRC bit (T1-ESF only).
Signalling_Location	O	Signal indicating location of Signalling bit.
FAW_Location	O	Signal indicating location of FAW bit.
A_Bit_Location	O	Signal indicating location of Alarm bit.
MF_Sync	O	Signal indicating end of multiframe.

Signal	Direction	Description
G.733 SPECIFIC SIGNALS Note: The T1 Deframer also produces delayed versions of these signals that are delayed by an integer number of data bit cycles, set through the Output_Delay input. Note that this delay must less than 1 frame (i.e. 192 max.)		
G733_M_Bit_Location	O	Signal indicating location of G.733 M (DL) bit.
G733_S_Bit_Location	O	Signal indicating location of G.733 S (Fs) bit.
G733_F_Bit_Location	O	Signal indicating location of all G.733 F bits.
ALARM & ERROR SIGNALS		
G733_Sync_Loss	O	G.733 Frame Synchronization Loss indicator.
G733_FAW_Errort_Count[3:0]	O	G.733 FAW error count
G733_Valid_FAW_Location	O	G.733 Valid FAW Location signal.
G733_Back_Alarm	O	G.733 Back Alarm status.

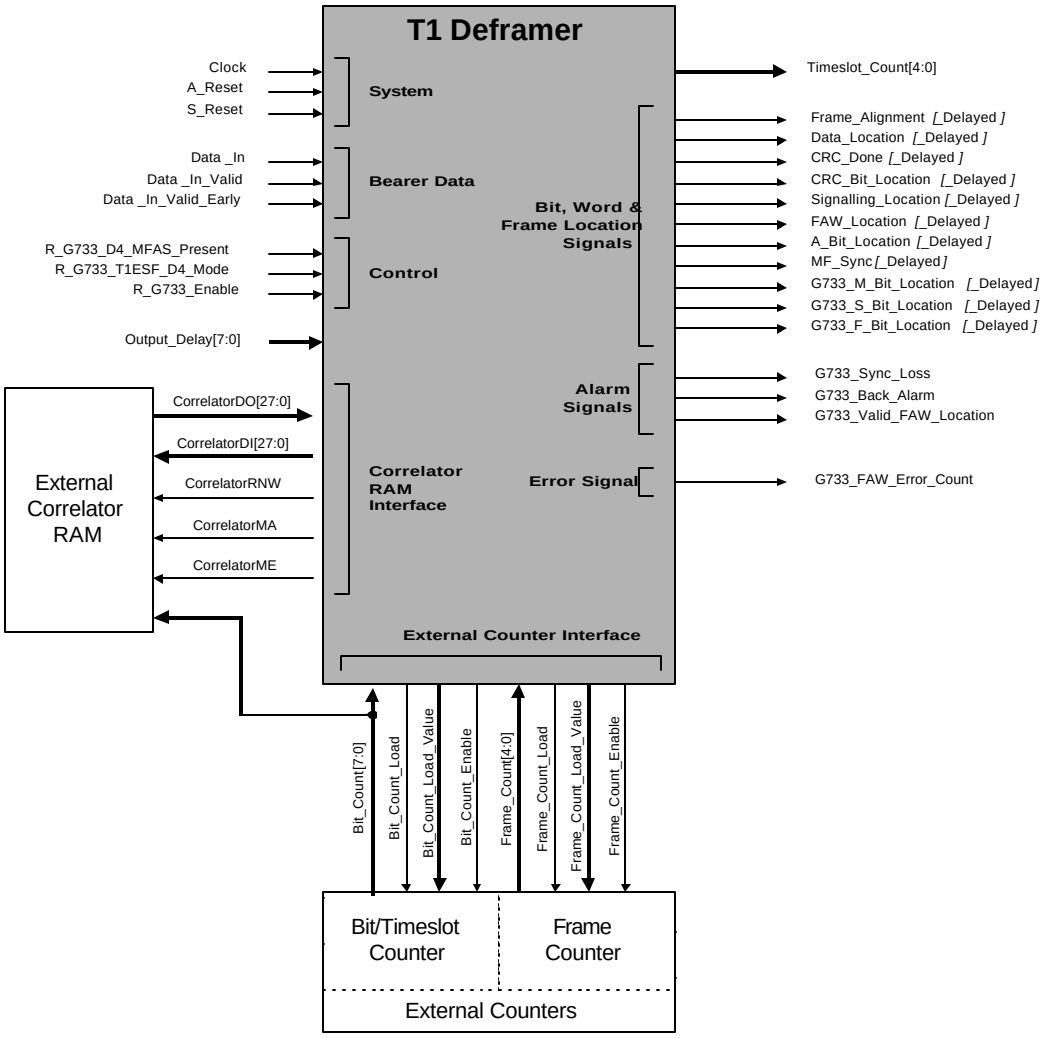


Figure 5: Core Schematic

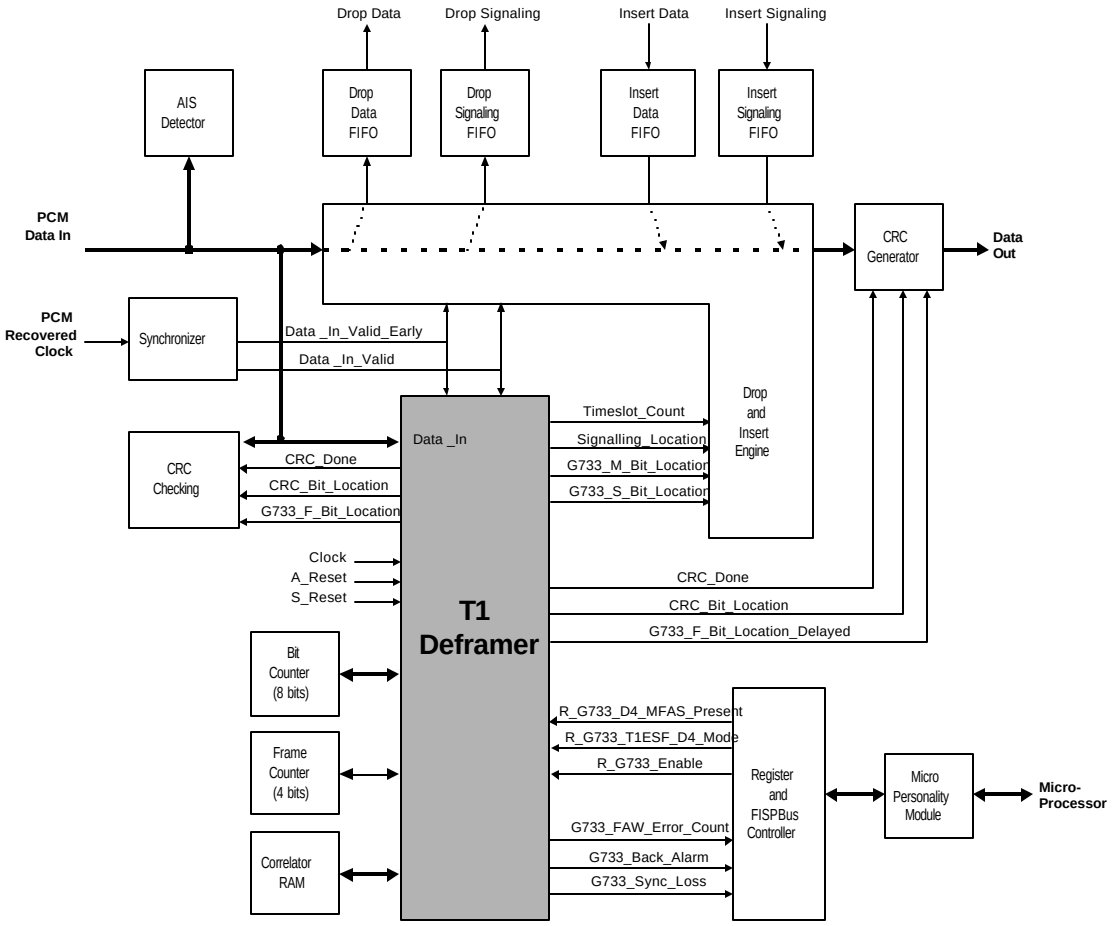
Example of Use

The diagram below shows how the T1 Deframer Core forms part of a system which can be used to drop and insert data octets. In the system illustrated below, the core is combined with a Drop and Insert Engine to allow all 32 data octets to be dropped and inserted every frame. If selective drop and insert is required, a Timeslot Re-orderer can be used. CRC checking and generation is done by the CRC block. A typical system is outlined in the following diagram which shows the T1 Deframer being used in conjunction with a basic drop and insert system and other standard elements.

Frame Alignment Method

Frame alignment is recovered using a proprietary technique based on correlation and statistical averaging. The framing algorithm maintains a table of Unconfirmed Framing Objects (UFOs) which are systematically eliminated as Frame Lock is achieved. This gives a compact solution that locks quickly enough to meet the framing requirements, and guarantees a frame acquisition time of under 15ms in 99.8% of all cases. The algorithm requires a RAM of 193 locations x 28 bits and a clock frequency of at least eight times the bearer rate (i.e. 8 x 1.544MHz).

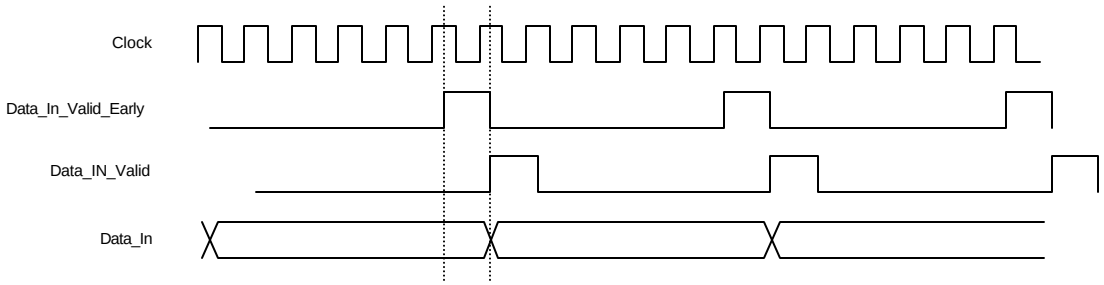
Figure 6: Example System



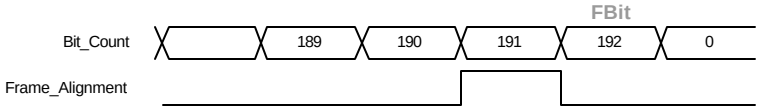
Timing Diagrams

Note: All signals have a delayed version in which the signal is delayed by a global integer number of data bit cycles (≤192).

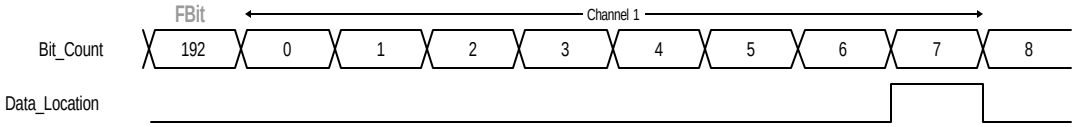
Data_In_Valid Timing



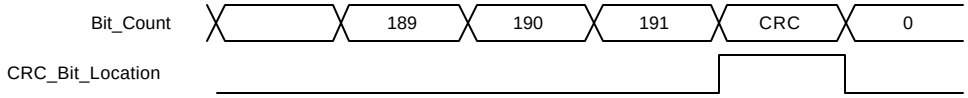
Frame Alignment Timing



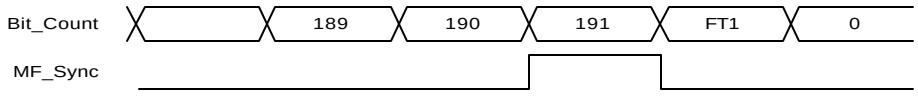
Data Location Timing



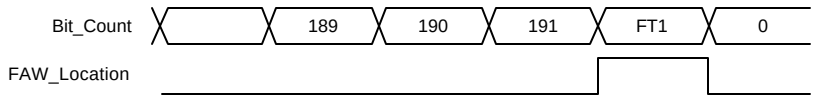
CRC_Bit_Location Timing



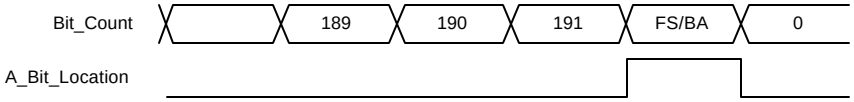
MF_Sync Timing



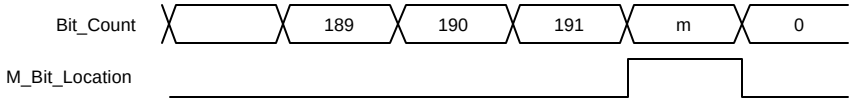
FAW_Location Timing



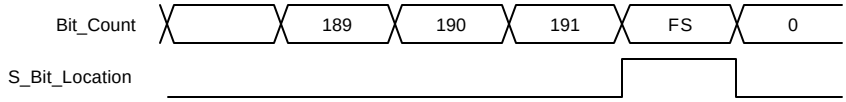
A-Bit_Location Timing



G733_M_Bit_Location Timing



G733_S_Bit_Location Timing



Frame Contents

The generated frames have the following contents:

T1 D4 Frame Structure (12 Frame)

Bit Count	F_Bit 192	TS0 0 7	TS1 8 15	TS2 16 23	TS3 24 31	TS4 32 39	TS5 40 47	TS6 48 55	TS7 56 63
Frame 0	FT 1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 1	FS 0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 2	FT 0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 3	FS 0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 4	FT 1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 5	FS 1	CH1 A	CH2 A	CH3 A	CH4 A	CH5 A	CH6 A	CH7 A	CH8 A
Frame 6	FT 0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 7	FS 1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 8	FT 1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 9	FS 1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 10	FT 0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 11	FS/BA	CH1 B	CH2 B	CH3 B	CH4 B	CH5 B	CH6 B	CH7 B	CH8 B
Bit Count		**TS8 64 71**	**TS9 72 79**	**TS10 80 87**	**TS11 88 95**	**TS12 96 103**	**TS13 104 111**	**TS14 112 119**	**TS15 120 127**
Frame 0		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 1		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 2		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 3		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 4		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 5		CH9 A	CH10 A	CH11 A	CH12 A	CH13 A	CH14 A	CH15 A	CH16 A
Frame 6		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 7		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 8		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 9		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 10		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 11		CH9 B	CH10 B	CH11 B	CH12 B	CH13 B	CH14 B	CH15 B	CH16 B
Bit Count		**TS16 128 135**	**TS17 136 143**	**TS18 144 151**	**TS19 152 159**	**TS20 160 167**	**TS21 168 175**	**TS22 176 183**	**TS23 184 191**
Frame 0		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 1		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 2		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 3		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 4		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 5		CH17 A	CH18 A	CH19 A	CH20 A	CH21 A	CH22 A	CH23 A	CH24 A
Frame 6		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 7		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 8		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 9		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 10		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 11		CH17 B	CH18 B	CH19 B	CH20 B	CH21 B	CH22 B	CH23 B	CH24 B

FT - Frame Alignment Word bit **FS - Signalling Frame Alignment** **FS/BA = 0 for FS, 1 for Back Alarm**

A, B - Robbed Bit Signalling bits **(NOT to CCITT Numbering Scheme)**

T1 ESF Frame Structure

Bit Count	F_Bit 192	TS0 0 7	TS1 8 15	TS2 16 23	TS3 24 31	TS4 32 39	TS5 40 47	TS6 48 55	TS7 56 63
Frame 0	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 1	CRC	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 2	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 3	FAW '0'	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 4	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 5	CRC	CH1 A	CH2 A	CH3 A	CH4 A	CH5 A	CH6 A	CH7 A	CH8 A
Frame 6	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 7	FAW '0'	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 8	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 9	CRC	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 10	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 11	FAW '1'	CH1 B	CH2 B	CH3 B	CH4 B	CH5 B	CH6 B	CH7 B	CH8 B
Frame 12	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 13	CRC	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 14	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 15	FAW '0'	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 16	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 17	CRC	CH1 C	CH2 C	CH3 C	CH4 C	CH5 C	CH6 C	CH7 C	CH8 C
Frame 18	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 19	FAW '1'	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 20	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 21	CRC	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 22	DL	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Frame 23	FAW '1'	CH1 D	CH2 D	CH3 D	CH4 D	CH5 D	CH6 D	CH7 D	CH8 D

Bit Count		TS8 64 71	TS9 72 79	TS10 80 87	TS11 88 95	TS12 96 103	TS13 104 111	TS14 112 119	TS15 120 127
Frame 0		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 1		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 2		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 3		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 4		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 5		CH9 A	CH10 A	CH11 A	CH12 A	CH13 A	CH14 A	CH15 A	CH16 A
Frame 6		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 7		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 8		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 9		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 10		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 11		CH9 B	CH10 B	CH11 B	CH12 B	CH13 B	CH14 B	CH15 B	CH16 B
Frame 12		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 13		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 14		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 15		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 16		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 17		CH9 C	CH10 C	CH11 C	CH12 C	CH13 C	CH14 C	CH15 C	CH16 C
Frame 18		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 19		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 20		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 21		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 22		CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
Frame 23		CH9 D	CH10 D	CH11 D	CH12 D	CH13 D	CH14 D	CH15 D	CH16 D

Bit Count		TS16 128 135	TS17 136 143	TS18 144 151	TS19 152 159	TS20 160 167	TS21 168 175	TS22 176 183	TS23 184 191
Frame 0		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 1		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 2		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 3		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 4		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 5		CH17 A	CH18 A	CH19 A	CH20 A	CH21 A	CH22 A	CH23 A	CH24 A
Frame 6		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 7		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 8		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 9		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 10		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 11		CH17 B	CH18 B	CH19 B	CH20 B	CH21 B	CH22 B	CH23 B	CH24 B
Frame 12		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 13		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 14		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 15		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 16		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 17		CH17 C	CH18 C	CH19 C	CH20 C	CH21 C	CH22 C	CH23 C	CH24 C
Frame 18		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 19		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 20		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 21		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 22		CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24
Frame 23		CH17 D	CH18 D	CH19 D	CH20 D	CH21 D	CH22 D	CH23 D	CH24 D

DL - Data Link bit CRC - CRC bit FAW - Frame Alignment Word bit A,B,C,D - Robbed Bit Signalling bits (NOT to CCITT Numbering Scheme)

Related Information

Copyright Information

The T1 Deframer module and associated files are proprietary, confidential information of Mentor Graphics Corporation. It is distributed by Xilinx, Inc. under license from Mentor Graphics Corporation and may only be used, copied and/or disclosed according to the terms of a valid license agreement with Xilinx, Inc.

Assumed Knowledge

It is assumed that the user is familiar with all aspects of HDL-based design flows from component instantiation in either Verilog or VHDL (and all other aspects of Verilog/VHDL syntax) to HDL simulation using test benches and script-based synthesis. It is also assumed that the user is familiar with the relevant telecommunication standards.

Installation Guidelines

To install the T1 Deframer design into the Xilinx Core Generator, copy the whole of the delivered directory structure to your $XILINX/coregen/ip/xilinx directory. Then call up Core Generator and ensure that the Mentor Graphics T1 Deframer module is listed among the Communications & Networking/Telecommunications modules. This will give you a $XILINX/coregen/ip/xilinx/t1_deframer/com/xilinx/ip/t1_deframer directory (hereafter referred to as your T1 Deframer product directory). The detailed structure of the delivered files is described in the readme text file included in your T1 Deframer product directory.

Note: While the cores based on Xilinx components can be generated in the same area as the source files, you are strongly recommended to create your project directory in a separate location. Similarly, if you want to use the supplied Chip Example, you should copy them out of the Core Generator tree before working on them.

Component Instantiation

The T1 Deframer module may be included in user designs by instancing the module as a component. Example declarations showing all the I/O port names are included in the templates provided in the virtex/templates directory within your T1 Deframer product directory. The example VHDL declaration is provided in the t1_deframer.vho file. The example Verilog declaration is provided in the t1_deframer.veo file.

Compilation Guidelines

An example compilation script is provided as the file xilrun.cmd (for Unix)/xilrun.bat (for DOS) in the virtex/chip_example/xilinx_run directory within your T1 Deframer product directory. These example compilation scripts process the example chip-level EDIF netlist provided alongside the xilrun.cmd and xilrun.bat files for a range of Xilinx implementation tools (ngdbuild, map and par) and the 'trce' timing report generation tool.

Synthesis Guidelines

For synthesis, the core should be declared as a 'black box' which will then be incorporated into your design during the translation stage of the synthesis process (provided the relevant netlist file can be found on the search path).

An unpadded EDIF description of the core may be found as an .edn file in the virtex/implement directory within your T1 Deframer product directory. Use this netlist along with the appropriate snippets from the t1_deframer.vho/.veo files to integrate the T1 Deframer into your design.

An example .ucf constraints file may be found in the virtex/chip_example/xilinx_run directory.

Simulation Guidelines

HDL test benches for use with the VHDL/Verilog descriptions of the core are provided, together with functional and post-layout simulation models and example compile-and-simulate scripts for use under ModelSim.

The functional simulation models are provided in the virtex/func_sim directory. Use the code snippets in the appropriate .vho/.veo template file to integrate these functional models into the functional simulation model for your design.

The post-layout simulation models, test benches and compile-and-simulate scripts are provided in the virtex/chip_example/verilog|vhdl directory, together with SDF files containing timing information. Each of these directories contains a modelsim.do file which runs the simulation test bench under ModelSim.

Test Bench and Test Data

The provided test benches do the following:

- Instantiate the core
- Generate input test vectors and apply them to the core
- Compare the output with expected 'golden' results
- Test the operation of reset and confirm that the expected values are selected
- Flag any mismatch between the actual output and the expected result of the simulation

Libraries

For simulation, it is assumed that the Xilinx-supplied 'simprims' and 'unisims' libraries have been compiled for use under ModelSim and stored in the $XILINX/verilog|vhdl/mti directory. Using the Xilinx-supplied Perl scripts will cause the correct libraries to be compiled.

Ordering Information

Xilinx LogiCORE modules are provided under Xilinx LogiCORE standard license agreement. For price and availability information, please contact your local Xilinx Sales Representative.