XCR3064XL 64 Macrocell CPLD

DS017 (v1.3) December 8, 2000 **Product Specification**

Features

- 6.0 ns pin-to-pin logic delays
- System frequencies up to 145 MHz
- 64 macrocells with 1,600 usable gates
- Available in small footprint packages
  - 44-pin PLCC (36 user I/O pins)
  - 44-pin VQFP (36 user I/O pins)
  - 48-ball CS BGA (40 user I/O pins)
  - 56-ball CP BGA (48 user I/O pins)
  - 100-pin VQFP (68 user I/O pins)
- Optimized for 3.3V systems
  - Ultra-low power operation
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five metal layer reprogrammable process
  - FZP™ CMOS design technology
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 available clocks per function block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per function block
- Fast ISP programming times
- Port Enable pin for dual function of JTAG ISP pins
- 2.7V to 3.6V supply voltage at industrial temperature range
- Programmable slew rate control per macrocell
- Security bit prevents unauthorized access
- Refer to XPLA3 family data sheet (DS012) for architecture description

Description

The XCR3064XL is a 3.3V, 64-macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of four function blocks provide 1,600 usable gates. Pin-to-pin propagation delays are 6.0 ns with a maximum system frequency of 145 MHz.

TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its sum of products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 1 and Table 1 showing the I_{CC} vs. Frequency of our XCR3064XL TotalCMOS CPLD (data taken with four up/down, loadable 16-bit counters at 3.3V, 25°C).

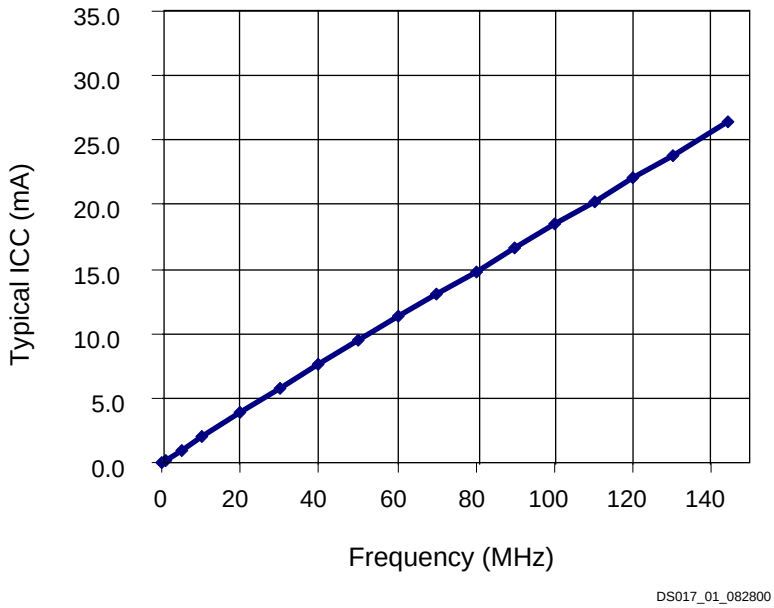


Figure 1: **I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C**

Table 1: **I_{CC} vs. Frequency** (V_{CC} = 3.3V, 25°C)

Frequency (MHz)	0	1	5	10	20	40	60	80	100	120	140
Typical I_{CC} (mA)	0	0.2	1.0	2.0	3.9	7.6	11.3	14.8	18.5	22.1	25.6

DC Electrical Characteristics Over Recommended Operating Conditions(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output High voltage for 3.3V outputs	I_{OH} = –8 mA	2.4	-	V
V_{OL}	Output Low voltage for 3.3V outputs	I_{OL} = 8 mA	-	0.4	V
I_{IL}	Input leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{IH}	I/O High-Z leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{CCSB}	Standby current	V_{CC} = 3.6V	-	100	µA
I_{CC}	Dynamic current(2,3)	f = 1 MHz	-	0.5	mA
		f = 50 MHz	-	15	mA
C_{IN}	Input pin capacitance(4)	f = 1 MHz	-	8	pF
C_{CLK}	Clock input capacitance(4)	f = 1 MHz	-	12	pF
$C_{I/O}$	I/O pin capacitance(4)	f = 1 MHz	-	10	pF

Notes:
1. See XPLA3 family data sheet (DS012) for recommended operating conditions.
2. See Table 1, Figure 1 for typical values.
3. This parameter measured with a 16-bit, loadable up/down counter loaded into every function block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
4. Typical values, not tested.

AC Electrical Characteristics Over Recommended Operating Conditions(1,2)

Symbol	Parameter	-6		-7		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{PD1}	Propagation delay time (single p-term)	-	5.5	-	7.0	-	9.1	ns
T_{PD2}	Propagation delay time (OR array)(3)	-	6.0	-	7.5	-	10.0	ns
T_{CO}	Clock to output (global synchronous pin clock)	-	4.0	-	5.0	-	6.5	ns
T_{SUF}(4)	Setup time fast	2.0	-	2.5	-	3.0	-	ns
T_{SU}(4)	Setup time	4.0	-	4.8	-	6.3	-	ns
T_{H}(4)	Hold time	0	-	0	-	0	-	ns
T_{WLH}(4)	Global Clock pulse width (High or Low)	2.5	-	3.0	-	4.0	-	ns
Tt_{PLH}(4)	P-term clock pulse width	4.0	-	5.0	-	6.0	-	ns
T_{R}(4)	Input rise time	-	20	-	20	-	20	ns
T_{L}(4)	Input fall time	-	20	-	20	-	20	ns
f_{SYSTEM}(4)	Maximum system frequency	-	145	-	119	-	95	MHz
T_{CONFIG}(4)	Configuration time(5)	-	20.0	-	20.0	-	20.0	µs
T_{POE}(4)	P-term OE to output enabled	-	7.5	-	9.3	-	11.2	ns
T_{POD}(4)	P-term OE to output disabled(6)	-	7.5	-	9.3	-	11.2	ns
T_{PCO}(4)	P-term clock to output	-	6.5	-	8.3	-	10.7	ns
T_{PAO}(4)	P-term set/reset to output valid	-	8.0	-	9.3	-	11.2	ns

Notes:
1. Specifications measured with one output switching.
2. See XPLA3 family data sheet (DS012) for recommended operating conditions.
3. See Figure 4 for derating.
4. These parameters guaranteed by design and/or characterization, not testing.
5. Typical current draw during configuration is 8 mA at 3.6V.
6. Output C_L = 5 pF.

Timing Model

The XPLA3 architecture follows a simple timing model that allows deterministic timing in design and redesign. The basic timing model is shown in Figure 2. One key feature of the XPLA3 CPLD is the ability to have up to 48 product term inputs into a single macrocell and maintain consistent timing. This is achieved through the use of a fully populated PLA (Programmable AND Programmable OR Array) which also has the ability to share product terms and only use the required amount of product terms per macrocell. There is a fast path (T_{LOGI1}) into the macrocell which is used if there is a single product term. The T_{LOGI2} path is used for multiple product term timing. For optimization of logic, the XPLA3 CPLD architecture includes a Fold-back NAND path (T_{LOGI3}). There is a fast input path to each macrocell if used as an Input Register (T_{FIN}). XPLA3 also includes universal control terms (T_{UDA}) that can be used for synchronization of the macrocell registers in different function blocks. There is also slew rate control and output enable control on a per macrocell basis.

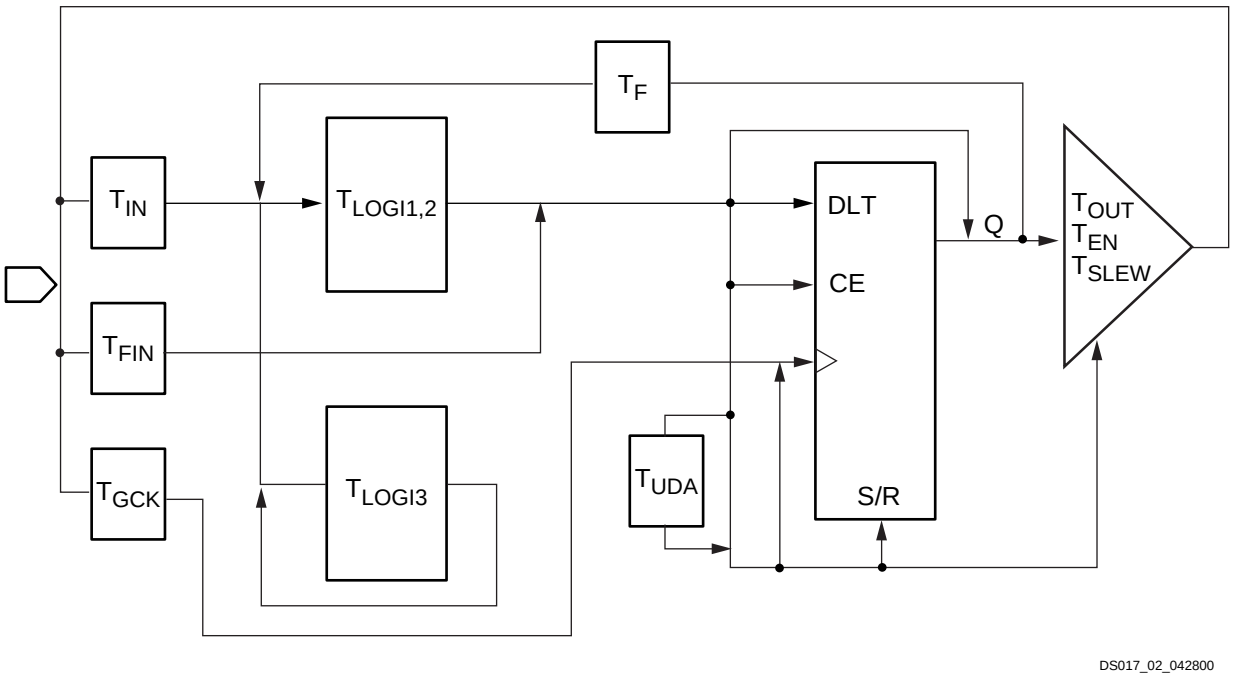


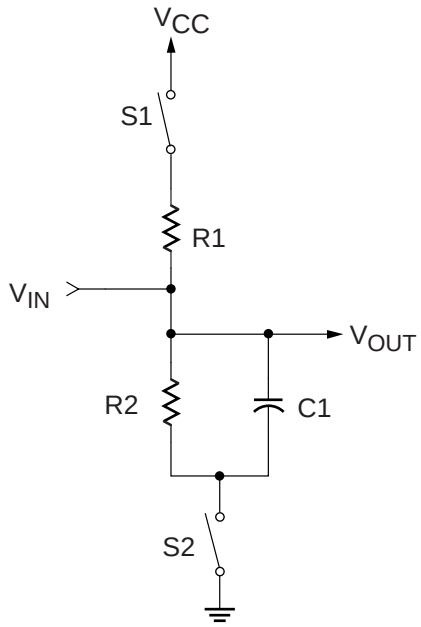
Figure 2: **XPLA3 Timing Model**

Internal Timing Parameters(1)

Symbol	Parameter	-6		-7		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Delays								
T_{IN}	Input buffer delay	-	1.3	-	1.6	-	2.2	ns
T_{FIN}	Fast Input buffer delay	-	1.8	-	2.5	-	3.1	ns
T_{GCK}	Global Clock buffer delay	-	0.8	-	1.0	-	1.3	ns
T_{OUT}	Output buffer delay	-	2.2	-	2.7	-	3.6	ns
T_{EN}	Output buffer enable/disable delay	-	4.2	-	5.0	-	5.7	ns
Internal Register and Combinatorial Delays								
T_{LDI}	Latch transparent delay	-	1.3	-	1.6	-	2.0	
T_{SUI}	Register setup time	1.0	-	1.0	-	1.2	-	ns
T_{HI}	Register hold time	4.0	-	5.5	-	6.7	-	ns
T_{ECSU}	Register clock enable setup time	2.0	-	2.5	-	3.0	-	ns
T_{ECHO}	Register clock enable hold time	3.0	-	4.5	-	5.5	-	ns
T_{COI}	Register clock to output delay	-	1.0	-	1.3	-	1.6	ns
T_{AOI}	Register async. S/R to output delay	-	2.5	-	2.3	-	2.1	ns
T_{RAI}	Register async. recovery	-	4.0	-	5.0	-	6.0	ns
T_{LOGI1}	Internal logic delay (single p-term)	-	2.0	-	2.7	-	3.3	ns
T_{LOGI2}	Internal logic delay (PLA OR term)	-	2.5	-	3.2	-	4.2	ns
Feedback Delays								
T_F	ZIA delay	-	2.4	-	2.9	-	3.5	ns
Time Adders								
T_{LOGI3}	Fold-back NAND delay	-	6.0	-	7.5	-	9.5	ns
T_{UDA}	Universal delay	-	1.5	-	2.0	-	2.5	ns
T_{SLEW}	Slew rate limited delay	-	4.0	-	5.0	-	6.0	ns

Notes:
1. These parameters guaranteed by design and/or characterization, not testing.

Switching Characteristics



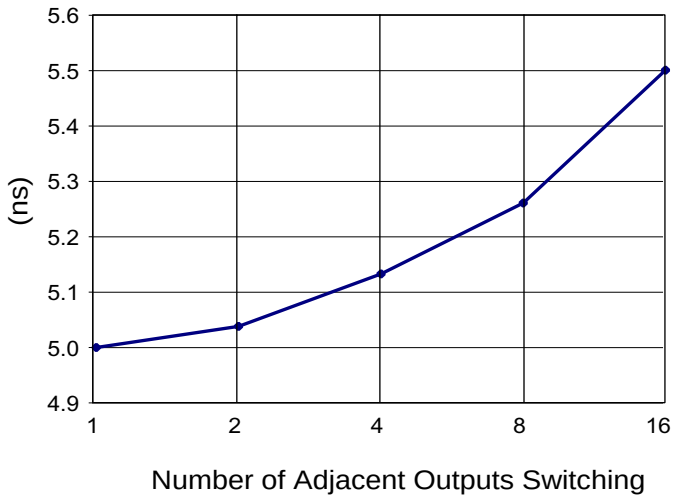
Component	Values
R1	390Ω
R2	390Ω
C1	35 pF

Measurement	S1	S2
T_{POE} (High)	Open	Closed
T_{POE} (Low)	Closed	Open
T_P	Closed	Closed

Note: For T_{POD}, C1 = 5 pF

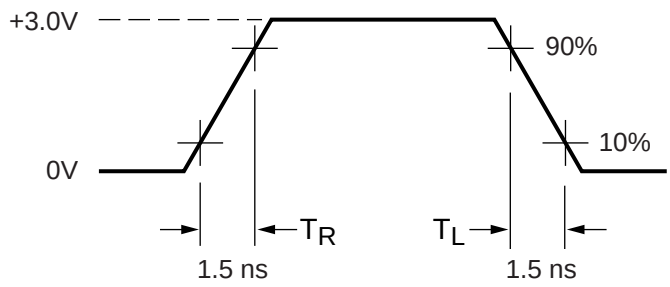
DS017_03_050200

Figure 3: **AC Load Circuit**



DS017_04_042800

Figure 4: **Derating Curve for T_{PD2}**



Measurements:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

DS017_05_042800

Figure 5: **Voltage Waveform**

Pin Descriptions

Table 2: **XCR3064XL I/O Pins**

Function Block	Macro-cell	PC44	VQ44	CS48	CP56	VQ100
1	1	41	35	C5	C8	85
1	2	40	34	A6	A8	84
1	3	-	-	-	-	83
1	4	-	-	-	A9	81
1	5	-	-	-	A5	80
1	6	-	-	A7	A10	79
1	7	-	-	-	-	76
1	8	39	33	B6	B10	75
1	9	38(1)	32(1)	B7(1)	C10(1)	73(1)
1	10	37	31	D4	D8	71
1	11	36	30	C6	E8	69
1	12	-	-	-	-	68
1	13	-	-	-	-	67
1	14	34	28	D6	F8	65
1	15	33	27	D7	E10	64
1	16	-	-	-	-	63
2	1	4	42	A2	C4	92
2	2	5	43	A1	C3	93
2	3	6	44	C4	A1	94
2	4	-	-	-	-	96
2	5	-	-	-	B1	97
2	6	-	-	-	-	98
2	7	-	-	-	A2	99
2	8	-	-	B2	A3	100
2	9	7(1)	1(1)	B1(1)	C1(1)	4(1)
2	10	8	2	C2	D1	6
2	11	9	3	C1	D3	8
2	12	-	-	-	-	9
2	13	-	-	-	-	10
2	14	11	5	D3	E3	12
2	15	12	6	D1	F1	13
2	16	-	-	-	-	14

Table 2: **XCR3064XL I/O Pins**

Function Block	Macro-cell	PC44	VQ44	CS48	CP56	VQ100
3	1	32(1)	26(1)	E5(1)	F10(1)	62(1)
3	2	31	25	E7	G8	61
3	3	-	-	-	-	60
3	4	29	23	F7	H10	58
3	5	-	-	-	-	57
3	6	-	-	-	-	56
3	7	-	-	F6	K8	54
3	8	-	-	-	K10	52
3	9	28	22	G7	K9	48
3	10	27	21	G6	J10	47
3	11	26	20	F5	H8	46
3	12	25	19	G5	H7	45
3	13	24	18	F4	H6	44
3	14	-	-	-	-	42
3	15	-	-	-	K7	41
3	16	-	-	-	-	40
4	1	13(1)	7(1)	D2(1)	G1(1)	15(1)
4	2	14	8	E1	F3	16
4	3	-	-	-	-	17
4	4	16	10	F1	G3	19
4	5	17	11	G1	J1	20
4	6	-	-	-	-	21
4	7	-	-	-	-	23
4	8	-	-	-	K1	25
4	9	18	12	E4	K4	29
4	10	19	13	F2	K2	30
4	11	20	14	G2	K3	31
4	12	21	15	F3	H3	32
4	13	-	-	G3	H4	33
4	14	-	-	-	-	35
4	15	-	-	-	K5	36
4	16	-	-	-	-	37

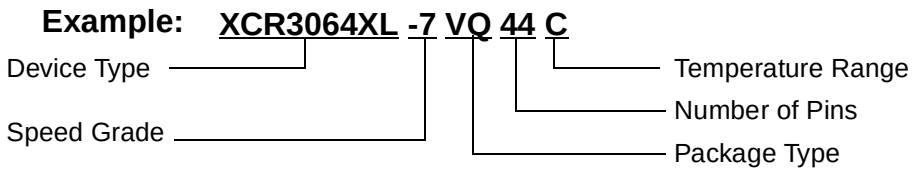
Notes:
1. JTAG pins

Table 3: **X36CR3064XL Global, JTAG, Port Enable, Power, and No connect Pins**

Pin Type	PC44	VQ44	CS48	CP56	VQ100
IN0 / CLK0	2	40	A3	C5	90
IN1 / CLK1	1	39	B4	C6	89
IN2 / CLK2	44	38	A4	C7	88
IN3 / CLK3	43	37	B5	A6	87
TCK	32	26	E5	F10	62
TDI	7	1	B1	C1	4
TDO	38	32	B7	C10	73
TMS	13	7	D2	G1	15
PORT_EN	10(1)	4(1)	C3(1)	E1(1)	11(1)
V_{CC}	3, 15, 23, 35	9, 17, 29, 41	B3, C7, E2, G4	A4, D10, H1, H5	3, 18, 34, 39, 51, 66, 82, 91
GND	22, 30, 42	16, 24, 36	A5, E3, E6	A7, G10, K6	26, 38, 43, 59, 74, 86, 95
No Connects	-	-	-	-	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78

Notes:
1. Port Enable is brought High to enable JTAG pins when JTAG pins are used as I/O. See family data sheet for more information.

Ordering Information



Device Ordering Options

Speed	
-10	10 ns pin-to-pin delay
-7	7.5 ns pin-to-pin delay
-6	6 ns pin-to-pin delay

Package	
PC44	44-pin Plastic Leaded Chip Carrier
VQ44	44-pin Very Thin Quad Flat Pack
CS48	48-ball Chip Scale Package
CP56	56-ball Chip Scale Package
VQ100	100-pin Very Thin Quad Flat Package

Temperature	
C = Commercial	T_A = 0°C to + 70°C V_{CC} = 3.0V to 3.6V
I = Industrial	T_A = –40°C to + 85°C V_{CC} = 2.7V to 3.6V

Component Availability

Pins		100	56	48	44	44
Type		Plastic VQFP	Plastic BGA	Plastic BGA	Plastic VQFP	Plastic PLCC
Code		VQ100	CP56	CS48	VQ44	PC44
XCR3064XL	-6	C	C	C	C	C
	-7, -10	C,I	C,I	C,I	C,I	C,I

Revision History

The following table shows the revision history for this document..

Date	Version	Revision
06/01/00	1.0	Initial Xilinx release.
08/30/00	1.1	Added 48-ball CS BGA package.
11/18/00	1.2	Updated to full production data sheet.
12/08/00	1.3	Added PC44 package.