# Reliability Testing Summary
# 0.22 µm

| | |
|---|---|
| **Technology:** | **Si Gate CMOS** |
| **Device Type:** | **XCVXXX** |
| **Package Type:** | **Various** |
| **Assumed Activation Energy:** | **0.70 ev @ C.L. = 60%** |

| | Life Test | Hast | Temp. Cycle |
|---|---|---|---|
| | 145C | 100 Hrs 130C/85% | 1,000Cycs. -65C/+150C |
| **Combined Lot:** | **21** | **1** | **1** |
| **Failures:** | **6** | **0** | **0** |
| **Device on test:** | **1,025** | **23** | **34** |
| **Actual device hours:** | **1,117,744** | **2,300** | **34,000** |
| **Mean:** | **1,090** | **100** | **1,000** |
| **Equivalent device hours @ Tj=125C:** | **2,967,035** | | |
| **Equivalent device hours @ Tj=70C:** | **230,903,313** | | |
| **Equivalent device hours @ Tj=25C:** | **2.79E+09** | | |
| **Failure Rate in FITS @ Tj=70C:** | **32** | | |
| **Failure Rate in FITS @ Tj=25C:** | **3** | | |

***The data collected from process qualification & Reliability monitor program**

**Dec. 29, 2000, Reliability Engineering**

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# Reliability Testing Summary
# 0.18 µm

| | |
|---|---|
| **Technology:** | **Si Gate CMOS** |
| **Device Type:** | **XCVXXXE** |
| **Package Type:** | **Various** |
| **Assumed Activation Energy:** | **0.70 ev @ C.L. = 60%** |

| | Life Test | Hast | Temp. Cycle |
|---|---|---|---|
| | 145C | 100Hrs 130C/85% | 1,000Cycs. -65C/+150C |
| **Combined Lot:** | **13** | **1** | **1** |
| **Failures:** | **2** | **0** | **0** |
| **Device on test:** | **500** | **76** | **68** |
| **Actual device hours:** | **318,156** | **7,600** | **68,000** |
| **Mean:** | **636** | **100** | **1,000** |
| **Equivalent device hours @ Tj=125C:** | **844,540** | | |
| **Equivalent device hours @ Tj=70C:** | **65,724,597** | | |
| **Equivalent device hours @ Tj=25C:** | **7.95E+08** | | |
| **Failure Rate in FITS @ Tj=70C:** | **47** | | |
| **Failure Rate in FITS @ Tj=25C:** | **4** | | |

***The data collected from process qualification & Reliability monitor program**

**Dec. 29, 2000, Reliability Engineering**

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