XCR3960: 960 Macrocell SRAM CPLD

DS032 (v1.3) October 9, 2000

Product Specification

Features

- Industry's largest CPLD–960 macrocells
- Industry's first SRAM-based CPLD
- Multiple configuration modes
  - Master serial
  - Slave serial
  - Master parallel-up
  - Slave parallel
  - Synchronous peripheral
  - In-system configurable through JTAG port
- Configuration times of under 1.0 second
- IEEE 1149.1 compliant JTAG testing capability
  - 5-pin JTAG interface
  - IEEE 1149.1 TAP controller
- 3.3V device
- Innovative XPLA2 Architecture combines extreme flexibility and high speeds
- Eight synchronous clock networks with programmable polarity at every macrocell
- Up to 96 asynchronous clocks support complex clocking needs
- Innovative XOR structure at every macrocell provides excellent logic reduction capability
- Logic expandable to 36 product terms on a single macrocell
- PCI compliant
- Advanced 0.35µ SRAM process
- Design entry and verification using industry standard and Xilinx CAE tools
- Innovative Control Term structure provides either sum terms of product terms in each logic block for:
  - 3-state buffer control
  - Asynchronous macrocell register reset/preset
- Global 3-state pin facilitates "bed of nails" testing without sacrificing logic resources
- Programmable slew rate control
- Small form factor 492-pin PBGA package provides 384 I/O pins
- Available in commercial and industrial temperature ranges

Description

The XCR3960 device is a member of the CoolRunner® family of high-density SRAM-based CPLDs (Complex Programmable Logic Device) from Xilinx. This device combines high-speed and deterministic pin-to-pin timing with high density. The XCR3960 uses the patented Fast Zero Power (FZP™) design technique that combines high speed and low power for the first time ever in a CPLD. FZP allows the XCR3960 to have true pin-to-pin timing delays of 7.5 ns, and standby currents of 100 µA without the need for "turbo bits" or other power-down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used since the bipolar era) with a cascaded chain of pure CMOS gates, both standby and dynamic power are dramatically reduced when compared to other CPLDs. The FZP design technique is also what allows Xilinx to offer a true CPLD architecture in a high-density device. Xilinx CoolRunner CPLDs are approximately twice the density and yet consume only half the power of standard CPLDs.

The Xilinx XCR3960 utilize the patented XPLA2 (eXtended Programmable Logic Array) architecture. This architecture combines the best features of both PAL- and PLA-type logic structures to deliver high-speed and flexible logic allocation that results in superior ability to make design changes with fixed pinouts. The XPLA2 architecture is constructed from 80 macrocell Fast Modules that are connected together by an interconnect array. Within each Fast Module are four Logic Blocks of 20 macrocells each. Each Logic Block contains a PAL structure with four dedicated product terms for each macrocell. In addition, each Logic Block has 32 additional product terms in a PLA structure that can be shared through a fully programmable OR array to any of the 20 macrocells. This combination efficiently allocates logic throughout the Logic Block, which increases device density and allows for design changes without redefining the pinout or changing the system timing. The XCR3960 offers pin-to-pin propagation delays of 7.5 ns through the PAL array of a Fast Module; and if the PLA array is used, an additional 1.5 ns is added to the delay, no matter how many PLA product terms are used. If the interconnect array between Fast Modules is used, there is a second fixed addition to the propagation delay of 4.0 ns. This means that the worst case pin-to-pin propagation delay within a fast module is 7.5 + 1.5 = 9.0 ns, and the delay from any pin to any other pin across the entire chip is 7.5 + 4.0 = 11.5 ns if only the PAL array is used, and 7.5 + 1.5 + 4.0 = 13.0 ns if the PLA array is used. This

deterministic timing allows you to establish system timing before the logic design is even started.

Each macrocell also has a two input XOR gate with the dedicated PAL product terms on one input and the PLA product terms on the other input. This patent-pending Versatile XOR structure allows for very efficient logic optimization compared to competing XOR structures that have only one product term as the second input to the XOR gate. The Versatile XOR allows an 8-bit XOR function to be implemented in only 20 product terms, compared to 65 product terms for the traditional XOR approach.

The XCR3960 is SRAM-based, which means that it is configured from an external source at power up by one of many different methods. The device may be reconfigured any number of times. See the configuration section of this data sheet for more information. The device supports the full JTAG specification (IEEE 1149.1) through an industry standard JTAG interface. It can also be configured through the JTAG port, which is very useful for prototyping. See “Device Configuration Through JTAG” on page 29. for more information.

The XCR3960 CPLDs are supported by industry standard CAE tools (Cadence/OrCAD, Exemplar Logic, Mentor, Synopsys, Synario, Viewlogic, and Synplicity), using text (ABEL, VHDL, Verilog) and/or schematic entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting uses a Xilinx developed tool including WebFITTER.

XPLA2 Architecture

Figure 1 shows a high-level block diagram of the XCR3960 implementing the XPLA2 architecture. The XPLA2 architecture is a multi-level, modular hierarchy that consists of Fast Modules interconnected by a virtual crosspoint switch called the Global Zero Power Interconnect Array (GZIA). Each Fast Module accepts 64 bits from the GZIA and outputs 64 bits to the GZIA. Each Fast Module is essentially an 80 macrocell CPLD with four logic blocks of 20 macrocells each inside. There are eight dedicated, low-skew, global clocks for the device; and each Fast Module has access to any two of these clocks (there are additional asynchronous clocks available in the Fast Modules, see Figure 3). There are also Global 3-state (GTS) and Global Reset (RSTN) pins that are common to all Fast Modules. When GTS is pulled High, all output buffers in the device will be disabled, causing all I/O pins to be 3-stated. When RSTN is pulled Low, all flip-flops of the device will be reset.

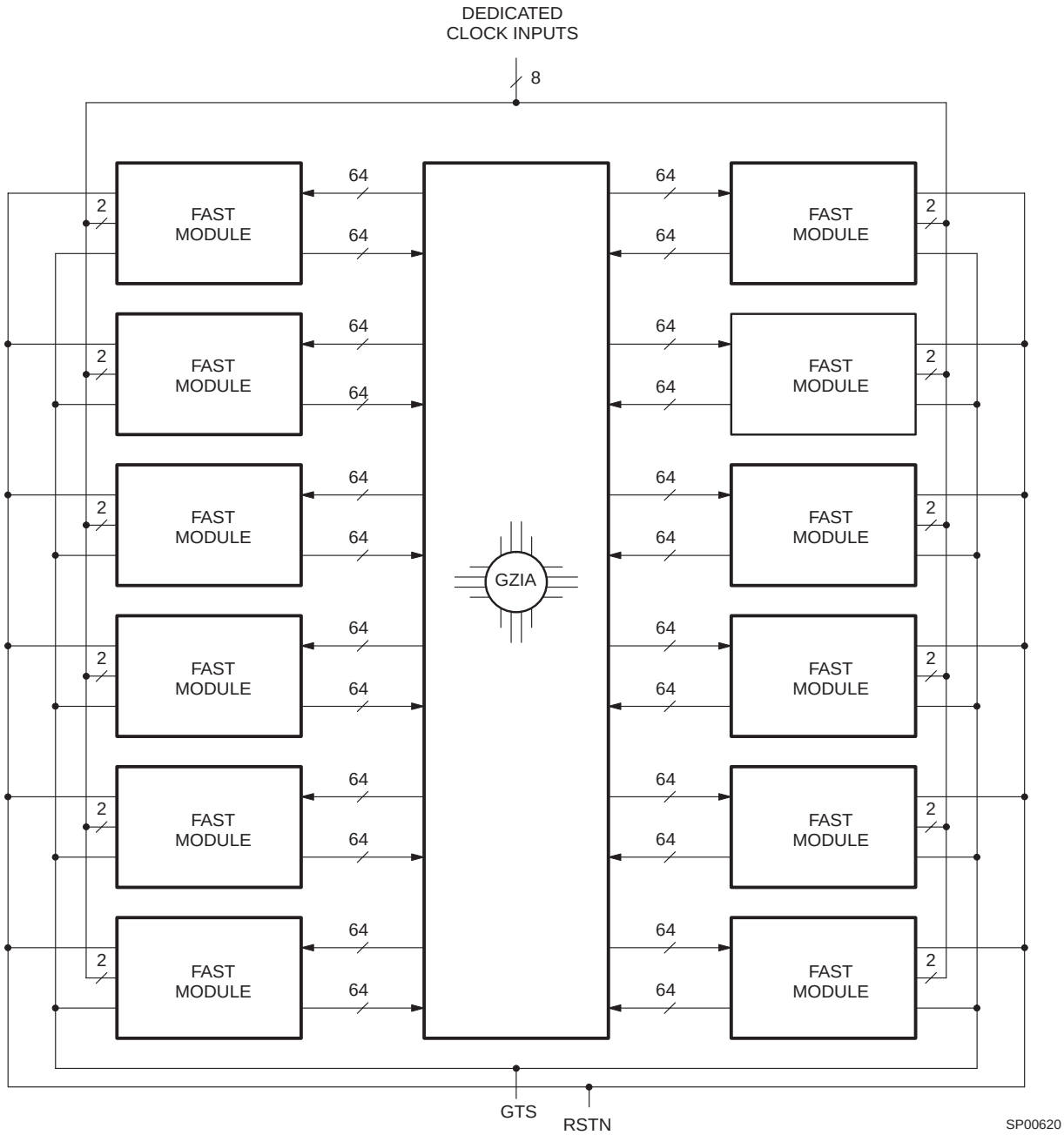


Figure 1: Xilinx XPLA2 CPLD Architecture

XPLA2 Fast Module

Each Fast Module (Figure 2) consists of four Logic Blocks of 20 macrocells each. Eight of the 20 macrocells in each Logic Block are connected to I/O pins and the remaining 12 can be used as buried nodes. These four Logic Blocks are connected together by the Local Zero Power Interconnect Array (LZIA). The LZIA is a virtual crosspoint switch that connects the Logic Blocks to each other and to the GZIA. The feedback from all 80 macrocells, input from the I/O pins, and the 64-bit input bus from the GZIA are input into the LZIA. The LZIA outputs 36 signals into each Logic Block and 64 signals into the GZIA.

XPLA2 Logic Block Architecture

Figure 3 illustrates the XPLA2 Logic Block architecture. Each Logic Block contains eight control terms, a PAL array, a PLA array, and 20 macrocells. The 36 inputs from the LZIA are available to all control terms and to each product term in both the PAL and the PLA array. The eight control terms can individually be configured as either SUM or PRODUCT terms, and are used to control the asynchronous preset and reset functions of the macrocell registers, the output enables of the 20 macrocells, and for asynchronous clocking. The PAL array consists of a programmable AND array with a fixed OR array, while the PLA array consists of a programmable AND array with a programmable OR array.

Each macrocell has four dedicated product terms from the PAL array. When additional logic is required, each macrocell takes the extra product terms from the PLA array. The PLA array consists of 32 extra product terms that are shared between the 20 macrocells of the Logic Block. The PAL product terms can be connected to the PLA product terms through either an OR gate or an XOR gate. One input to the XOR gate can be connected to all the PLA terms, which provides for extremely efficient logic synthesis. An 8-bit XOR function can be implemented in only 20 product terms. Each macrocell can use the output from the OR gate or the XOR gate in either normal or inverted state.

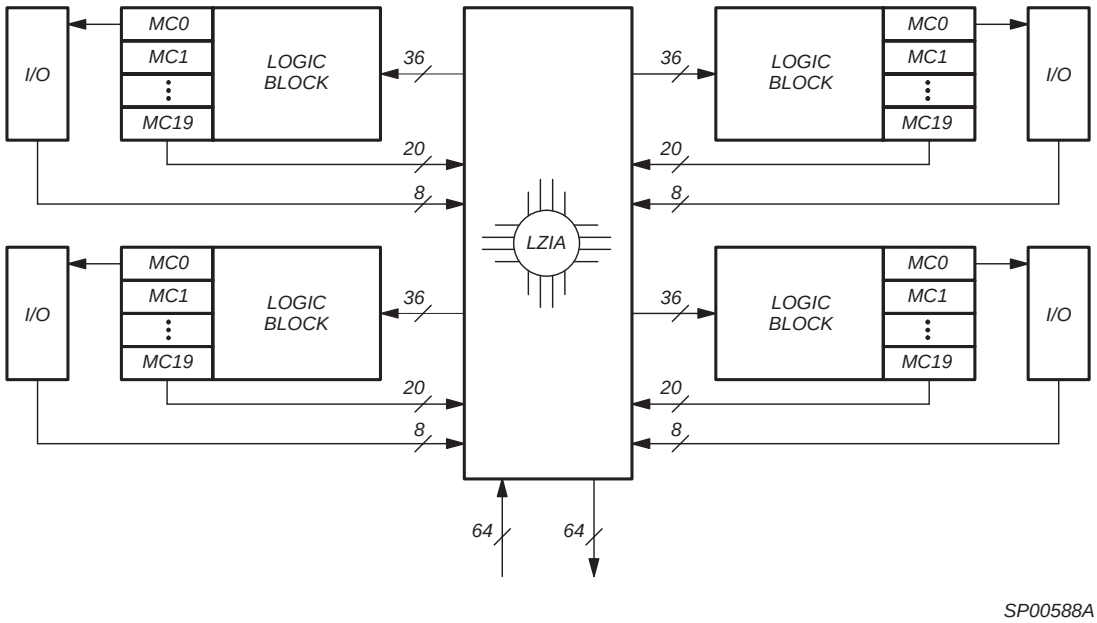


Figure 2: Xilinx XPLA2 Fast Module

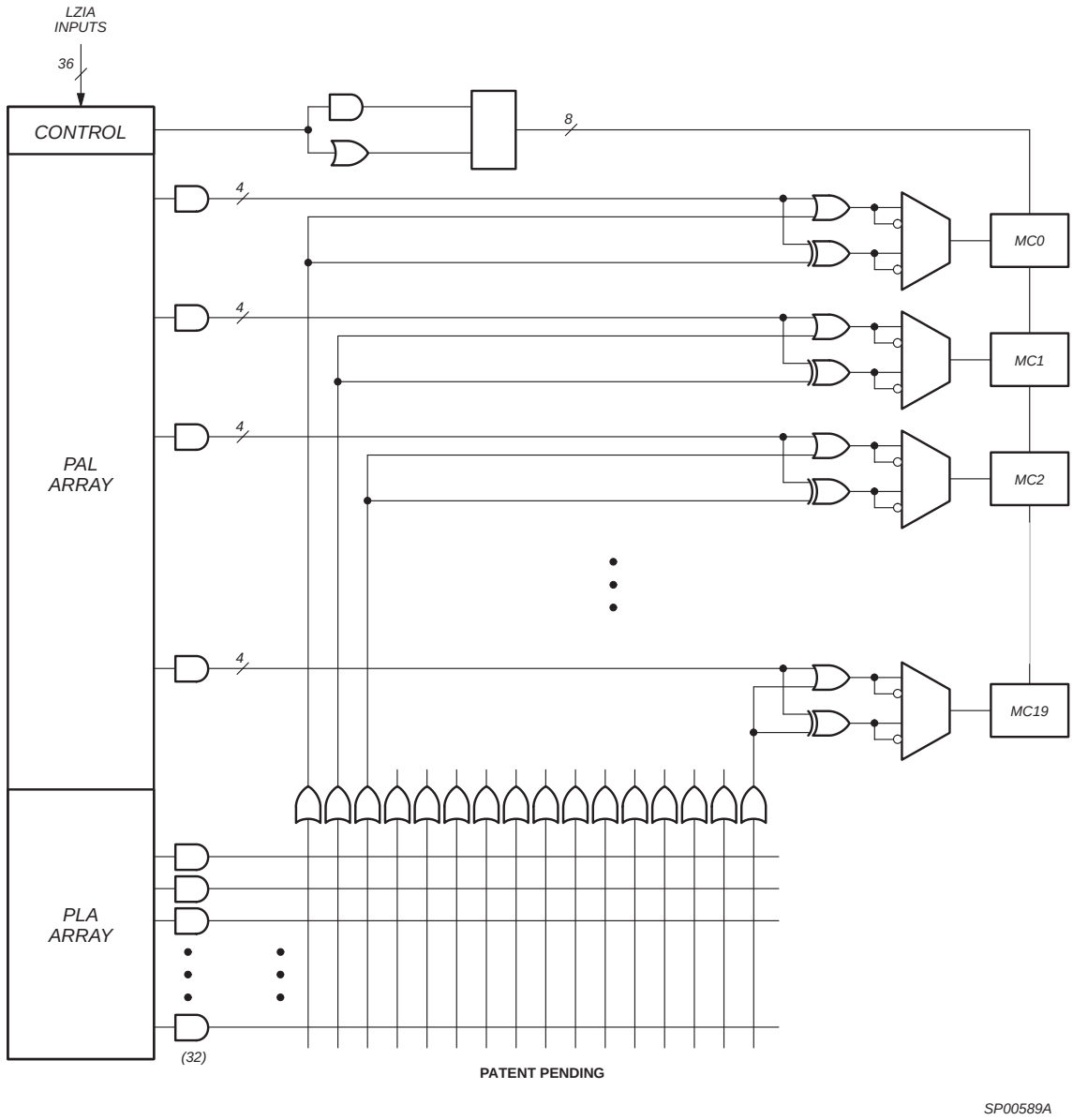


Figure 3: Xilinx XPLA2 Logic Block Architecture

XPLA2 Macrocell Architecture

Figure 4 shows the XPLA2 macrocell architecture used in the XCR3960. The macrocell can be configured as either a D- or T-type flip-flop or a combinatorial logic function. A D-type flip-flop is generally more useful for implementing state machines and data buffering while a T-type flip-flop is generally more useful in implementing counters. Each of these flip-flops can be clocked from any one of four sources. Two of the clock sources (CLK0 and CLK1) are from the eight dedicated, low-skew, global clock networks designed to preserve the integrity of the clock signal by reducing skew between rising and falling edges. These clocks are designated as a "synchronous" clocks and must be driven by an external source. Both CLK0 and CLK1 can clock the macrocell flip-flops on either the rising edge or the falling edge of the clock signal. The other clock sources are designated as "asynchronous" and are connected to two of the eight control terms (CT6 and CT7) provided in each Logic Block. These clocks can be individually configured as any PRODUCT term or SUM term equation created from the 36 signals available inside the logic block. Thus, in each Logic Block, there are up to four possible clocks; and in each Fast Module, there are up to ten possible clocks. Throughout the entire device, there are up to 104 possible clocks–eight from the dedicated, low-skew, global clocks, and two for each of the 48 logic blocks.

The remaining six control terms of each logic block (CT0-CT5) are used to control the asynchronous preset/reset of the flip-flops and the enable/disable of the output buffers in each macrocell. Control terms CT0 and CT1 are used to control the asynchronous preset/reset of the macrocell's flip-flop. Note that the power-on reset leaves all macrocells in the "zero" state when power is properly applied, and that the preset/reset feature for each macrocell can also be disabled. Each macrocell can choose between an asynchronous reset or an asynchronous preset function, but both cannot be simultaneously used on the same register. The global RSTN function can always be used, regardless of whether or not asynchronous reset or preset control terms are enabled. Control terms CT2, CT3, CT4, and CT5 are used to enable or disable the macrocell's output buffer. Having four dedicated output enable control terms ensures that the CoolRunner devices are PCI compliant. The output buffers can also be always enabled or always disabled. All CoolRunner devices also provide a Global 3-State (GTS) pin, which, when pulled High, will 3-state all the outputs of the device. This pin is provided to support "In-Circuit Testing" or "Bed-of-Nails" testing used during manufacturing.

For the macrocells in the Logic Block that are associated with I/O pins, there are two feedback paths to the LZIA: one from the macrocell, and one from the I/O pin. The LZIA feedback path before the output buffer is the macrocell feedback path, while the LZIA feedback path after the output buffer is the I/O pin feedback path. When these macrocells are used as outputs, the output buffer is enabled, and either feedback path can be used to feedback the logic implemented in the macrocell. When the I/O pins are used as inputs, the output buffer of these macrocells will be 3-stated and the input signal will be fed into the LZIA via the I/O feedback path. In this case the logic functions implemented in the buried macrocell can be fed back into the LZIA via the macrocell feedback path. For macrocells that are not associated with I/O pins, there is one feedback path to the LZIA. Logic functions implemented in these buried macrocells are fed back into the LZIA via this path. All unused inputs and I/O pins should be properly terminated. (See "Terminations" on page 8.)

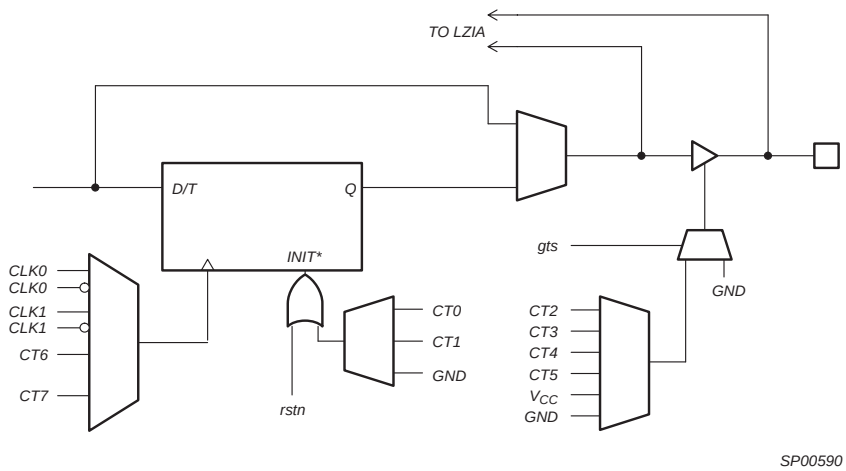


Figure 4: XCR3960 Macrocell Architecture

Simple Timing Model

Figure 5 shows the XCR3960 timing model. The XCR3960 timing model is very simple compared to the models of competing architectures. There are three main timing parameters: the pin-to-pin delay for combinatorial logic functions (t_{PD}), the input pin to register set-up time (t_{SU}), and the register clock to valid output time (t_{CO}). As the model shows, timing is only dependent on whether or not you use the PLA array, and whether or not the logic function is created within a single Fast Module or uses the GZIA. The timing starts with a set time for t_{PD} and t_{SU} through the PAL array in a Fast Module, and there are fixed delays added for use of the PLA array or the GZIA. The t_{CO} timing specification never changes. For example, a combinatorial logic function of four or fewer product terms constructed from inputs within the same Logic block would have a t_{PD} delay of 7.5 ns. If the logic function were more than four product terms wide, the delay would be t_{PD} plus the fixed PLA delay, or 7.5 + 1.5 = 9.0 ns. A function that used the PAL array and inputs from a different Fast Module would have a propagation delay of t_{PD} plus the fixed GZIA delay, or 7.5 + 4.0 = 11.5 ns.

This simple timing model allows designers to determine whether or not the device will meet system timing specifications up front. In competing devices, the user is unable to determine if the design will meet system timing requirements until after the design has been fit into the device. This is because the timing models of competing architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, the fan-out of a signal, the varying number of X and Y routing channels used, etc. The simplicity of the XCR3960 timing model gives you pin-to-pin delay information before the design is set. Further, the timing in the XCR3960 device will not vary with place and route iterations caused by design changes. This allows the XCR3960 device to meet your timing requirements even when you make changes to the design.

TotalCMOS™ Design Technique for FastZero Power

Xilinx is the first to offer a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its product terms instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs which are both high-performance and low power, breaking the paradigm that to have low power, you must have low performance. This also makes it possible to manufacture high-density CPLDs like the XCR3960 that consume a fraction of the power of competing devices. Refer to Figure 6 and Table 1 showing the I_{CC} vs. Frequency of the XCR3960 TotalCMOS CPLD (data taken with 60 16-bit counters at 3.3V, 25°C).

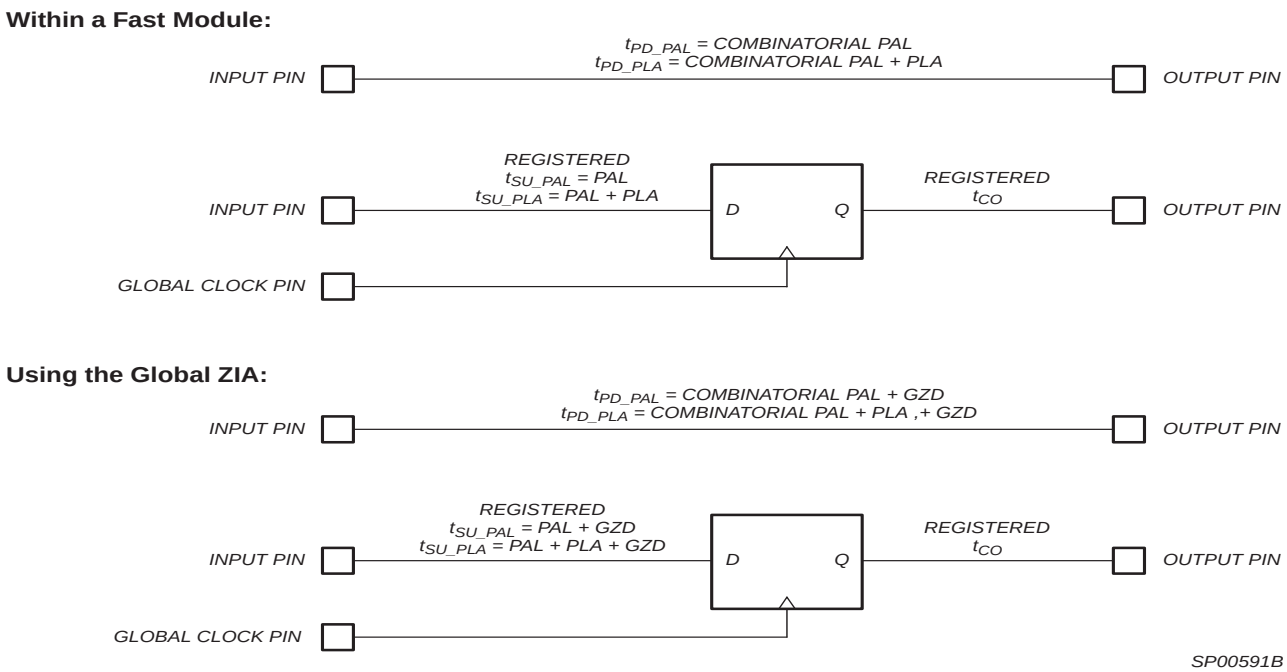


Figure 5: XCR3960 Timing Model

Table 1: I_{CC} vs. Frequency (V_{CC} = 3.3V, 25°C)

FREQUENCY (MHz)	0	1	20	40	60	80	100	120
Typical I_{CC} (mA)	0.1	4.1	76.7	150.1	222.2	294.6	364	441.6

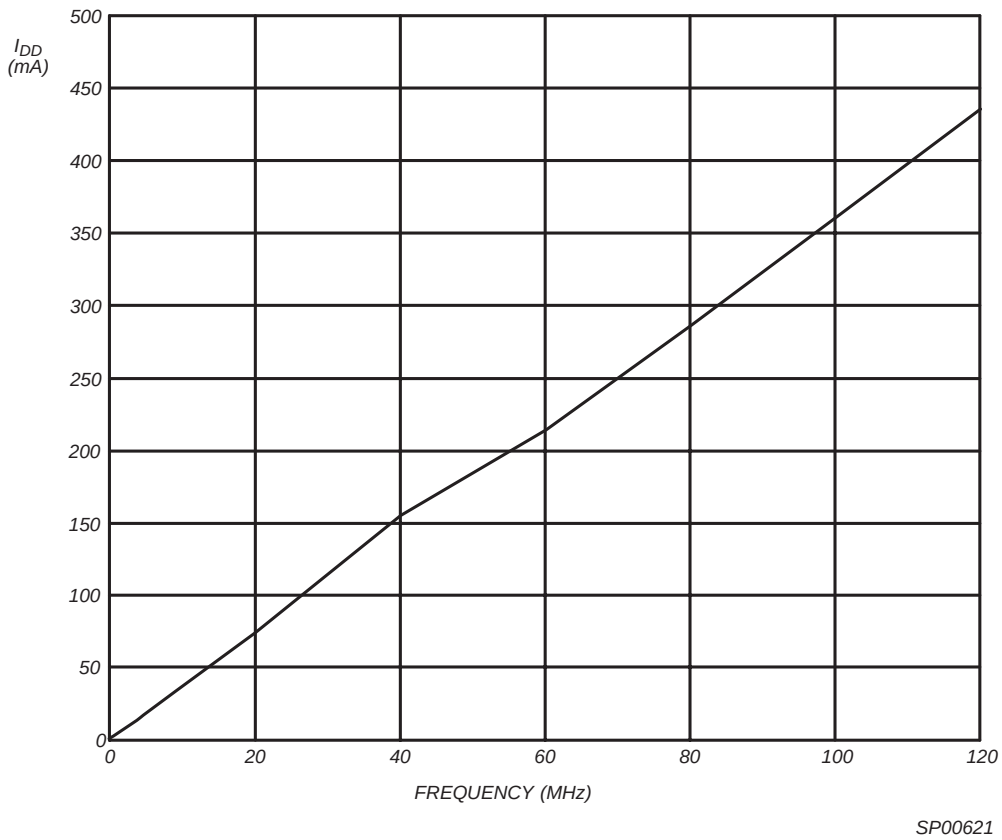


Figure 6: I_{CC} vs. Frequency @ V_{CC} = 3.3V, 25°C

Terminations

The CoolRunner XCR3960 CPLDs are TotalCMOS devices. As with other CMOS devices, it is important to consider how to properly terminate unused inputs and I/O pins when fabricating a PC board. Allowing unused inputs and I/O pins to float can cause the voltage to be in the linear region of the CMOS input structures, which can increase the power consumption of the device. It can also cause the voltage on a configuration pin to float to an unwanted voltage level, interrupting device operation.

The XCR3960 CPLDs have programmable on-chip pull-down resistors on each I/O pin. These pull-down resistors are only available for unused I/O pins, and are automatically activated by the fitter software. Note that an I/O macrocell used as buried logic that does not have the I/O pin used for input is considered to be unused, and the pull-down resistors will be turned on. It is recommended that any unused I/O pins on the XCR3960 device be left unconnected.

There are no on-chip pull-down structures associated with dedicated pins used for device configuration or special device functions like Global Reset and Global 3-state. Xilinx recommends that these pins be terminated consistent with the description given in Table 15. Xilinx recommends the use of weak pull-up and pull-down resistors for terminating these pins. See the appropriate configuration section for more information on terminating dedicated pins.

When using the JTAG Boundary Scan functions, it is recommended that 10 KΩ pull-up resistors be used on the TDI, TMS, TCK, and TRSTN pins. The TDO signal pin can be left floating unless it is connected to the TDI of another device. Letting these signals float can cause the voltage on TMS to come close to ground, which could cause the device to enter JTAG/ISP mode at unspecified times.

Configuration Introduction

The Xilinx CoolRunner series are available in technologies which use non-volatile (EEPROM-based) and volatile (SRAM based) configuration memory. The functionality of the XPLA2 family of the CoolRunner series is defined by on-chip SRAM. The devices are configured in a manner similar to that of most FPGAs. This section describes the configuration of the XCR3960, and applies to all similarly configured devices to be produced by Xilinx.

Either Xilinx or third party software is used to generate a JEDEC file. The JEDEC file contains the configuration data, which is loaded into the XCR3960 configuration memory to control the XCR3960 functionality. This is done at power-up and/or with configure command. This section provides some of the trade-offs in selecting a configuration mode, and provides debug hints for configuration problems.

There are several different methods of configuring the XCR3960. The mode used is selected using the mode select pins. There are three basic configuration methods: master, slave, and peripheral. The configuration data can be transmitted to the XCR3960 serially or in parallel bytes. As a master, the XCR3960 generates the clock and control signals to strobe configuration data into the XCR3960. As a slave device, a clock is generated externally, and provided into the XCR3960's CCLK pin. In the peripheral mode, the XCR3960 interfaces as a microprocessor peripheral. Note that M3 should always be High. Table 2 lists the states for the other mode pins, by configuration mode.

Table 2: Configuration Modes

M2	M1	M0	CCLK	Configuration Mode	Data Format
0	0	0	Output	Master serial	Serial
0	0	1	Input	Slave parallel	Parallel
0	1	0	Reserved		
0	1	1	Input	Synchronous peripheral	Parallel
1	0	0	Output	Master parallel-up	Parallel
1	0	1	Reserved		
1	1	0	Reserved		
1	1	1	Input	Slave serial	Serial

Design Flow Overview

Figure 7 is a diagram of the steps used in configuring the XCR3960. The development system is used to generate configuration data in the JEDEC file. Using the `<design>.jed` file, there are two general methods of configuring the XCR3960. The utility `download` can load the configuration data from a PC or workstation hard disk into the XCR3960. Alternately, the XCR3960 can be loaded from non-volatile ICs such as serial or parallel EEPROMs, after converting the JEDEC file to an MCS file using the `jed2mcs` utility.

XCR3960 States Of Operation

Prior to becoming operational, the XCR3960 goes through a sequence of states, including initialization, configuration, and start-up. This section discusses these three states. In the master configuration modes, the XCR3960 is the source of configuration clock (CCLK).

When configuration is initiated, a counter in the XCR3960 is set to 0 and begins to count configuration clock cycles applied to the XCR3960. As each configuration data frame is supplied to the XCR3960, it is internally assembled into data words. Each data word is loaded into the internal configuration memory. The configuration loading process is complete when the internal length count equals the loaded length count in the length count field, and the required end of configuration frame is written.

All configuration I/Os used as inputs operate with TTL-level input thresholds during configuration. All I/Os that are not used during the configuration process are 3-stated with internal pull-downs. During configuration, registers are reset. The combinatorial logic begins to function as the XCR3960 is configured. Figure 8 gives the general timing information for configuring the device. Figure 9 shows the flow between the initialization, configuration, and start-up states. Table 3 shows the general configuration mode timing characteristics.

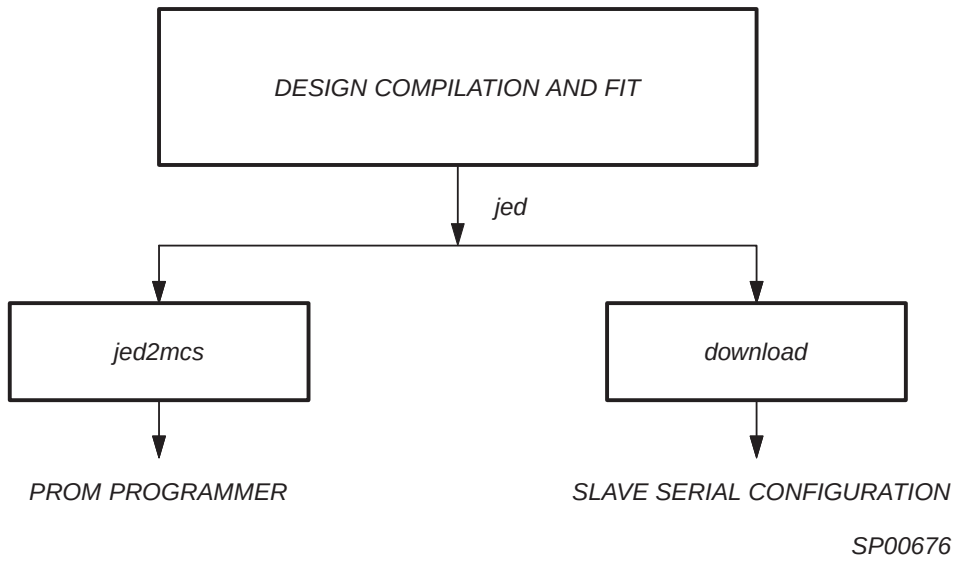


Figure 7: Design Flow

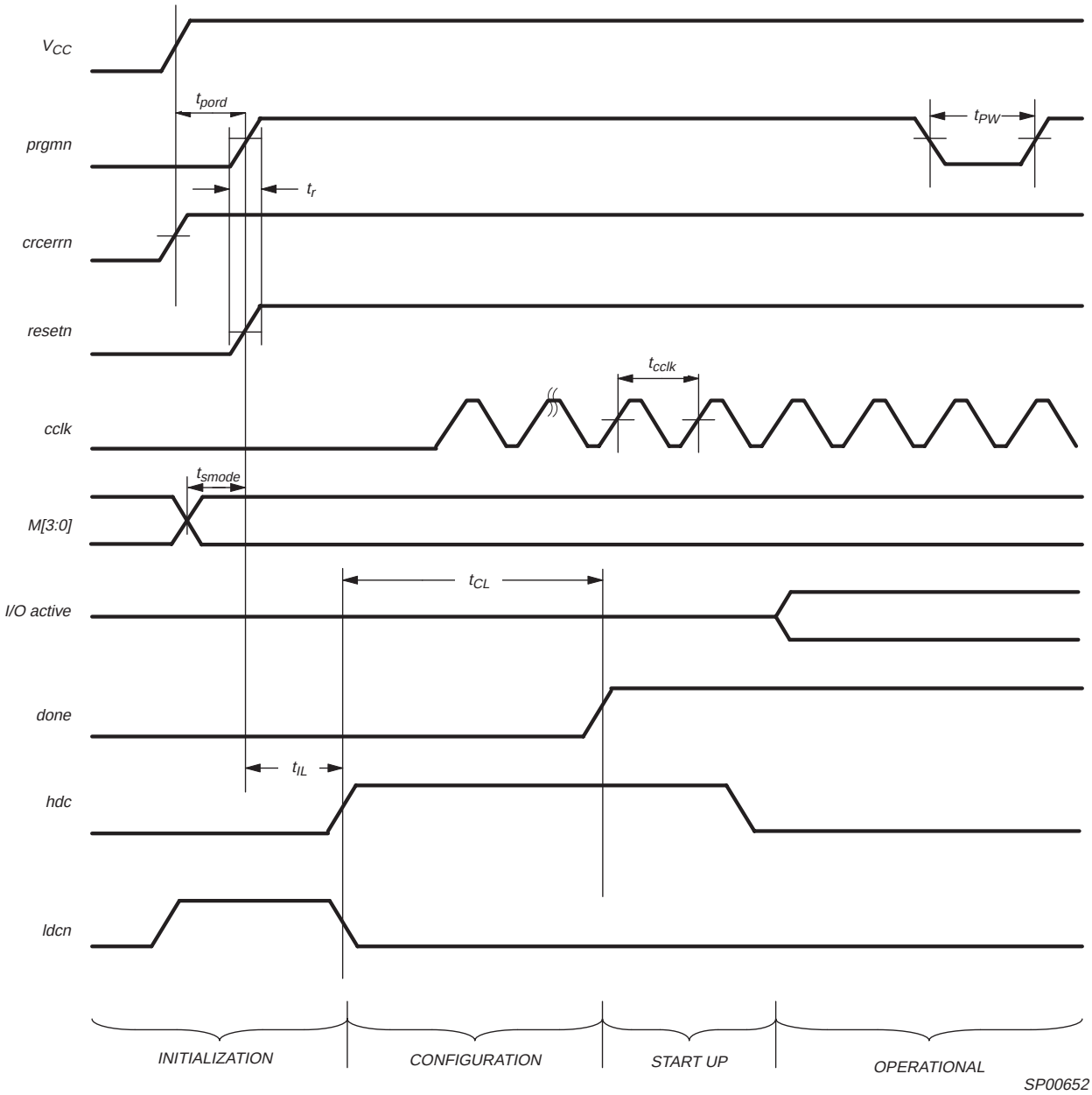


Figure 8: General Configuration Mode Timing Diagram

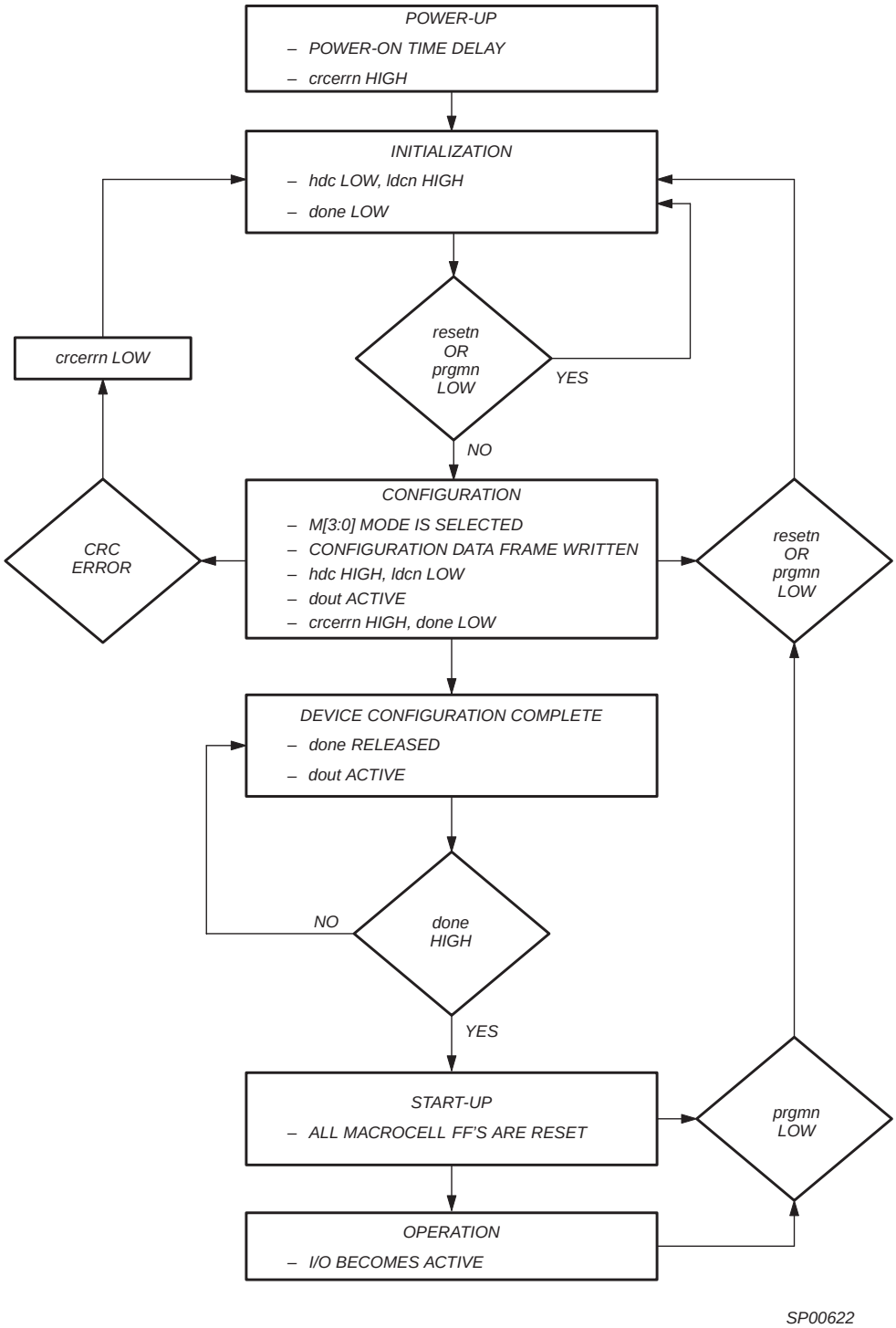


Figure 9: Flow Chart of Initialization, Configuration, and Operating States

Table 3: General Configuration Mode Timing Characteristics

Symbol	Parameter		Min	Max	Unit
All configuration modes					
t_{SMODE}	M[3:0] setup time to PRGMN High		0		ns
t_{HMODE}	M[3:0] hold time from DONE High		10		µs
t_{PW}	PRGMN pulse width Low		50		ns
t_{gtsr}	Global 3-state disable			40	ns
t_{IL}	Initialization latency (PRGMN High to HDC High) XCR3960	M3 = 1	250	700	ns
t_{PORD}	Power-on reset delay		1		µs
t_r	Configuration signal rise time			1.0	µs
Master modes					
t_{CCLK}	CCLK period	M3 = 1	714	1667	ns
t_{CL}	Configuration latency (non-compressed) XCR3960	M3 = 1	404	943	ms
Slave serial, slave parallel, and synchronous peripheral modes					
t_{CCLK}	CCLK period	Single device	100		ns
		Daisy chain	1000		ns
t_{CL}	Configuration latency (non-compressed) XCR3960	Single device	57		ms
		Daisy chain	566		ms

Initialization

Upon power-up, the device goes through an initialization process. First, an internal power-on-reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the XC3960 begin to operate (1.5V), the configuration pins are set to be inputs or outputs based on the configuration mode, as determined by the mode select inputs M[2:0]. The mode pins must be stable t_{SMODE} nanoseconds before the rising edge of PRGMN or RESETN. A time-out delay is initiated when V_{CC} reaches between 1.0V and 2.0V to allow the power supply voltage to stabilize. The DONE output is Low. At power-up, if the power supply does not rise from 1.0V to V_{CC} in less than 25 ms, the user should delay configuration by inputting a low into PRGMN or RESETN until V_{CC} is greater than the recommended minimum operating voltage (3.0V for commercial devices). If PRGMN has a rise time of greater than 1 µs, RESETN must be held Low until after PRGMN goes High. If the rise time for PRGMN is 1 µs or less, the order in which these pins go High is arbitrary.

The High During Configuration (HDC), Low During Configuration (LDCN), and done signals are active outputs in the XCR3960s initialization and configuration states. HDC, LDCN, and DONE can be used to provide control of external logic signals such as reset, bus enable, or EEPROM enable during configuration. For master parallel configuration mode, these signals provide EEPROM enable control and allow the data pins to be shared with user logic signals.

If configuration has begun, an assertion of RESETN or PRGMN initiates an abort, returning the XCR3960 to the initialization state. The RESETN and PRGMN pins must be High before the XCR3960 will enter the configuration state, and the mode pins must be stable t_{SMODE} ns before they rise. During the start-up and operating states, only the assertion of PRGMN causes a reconfiguration.

During initialization and configuration, all I/Os are 3-stated and the internal weak pull-downs are active. See “Terminations” on page 8.

Start-up

After configuration, the XCR3960 enters the start-up phase. This phase is the transition between the configuration and operational states. This transition occurs within three CCLK cycles of the DONE pin going High (it is acceptable to have additional CCLK cycles beyond the three required). The system design task in the start-up phase is to ensure that multi-function pins (See “Pinouts for XCR3960” on page 36.) transition from configuration signals to user definable I/Os without inadvertently activating devices in the system or causing bus contention. The done signal goes High at the beginning of the start-up phase, which allows configuration sources to be disconnected so that there is no bus contention when the I/Os become active. In addition to controlling the XCR3960 during start-up, additional start-up techniques to avoid contention include using isolation devices between the XCR3960 and other circuits in the system, reassigning I/O locations, and

keeping I/Os 3-stated until contentions are resolved. For example, Figure 10 shows how to use the Global 3-state (GTS) signal to avoid signal contention when any multi-function pins are used as I/O after configuration is finished. Holding GTS High until after the multi-function pins are disconnected from the driving source allows these pins to transition from configuration pins to user definable I/O without signal contention. In this case, the I/O become active a t_{GTSR} delay after the GTS pin is pulledLow.

The flip-flops are reset one cycle after done goes High so that operation begins in a known state. The DONE outputs from multiple XCR3960s can be wire ANDed and used as an active High ready signal, to disable PROMs with active Low enable(s), or to reset to other parts of the system (see Figure 27).

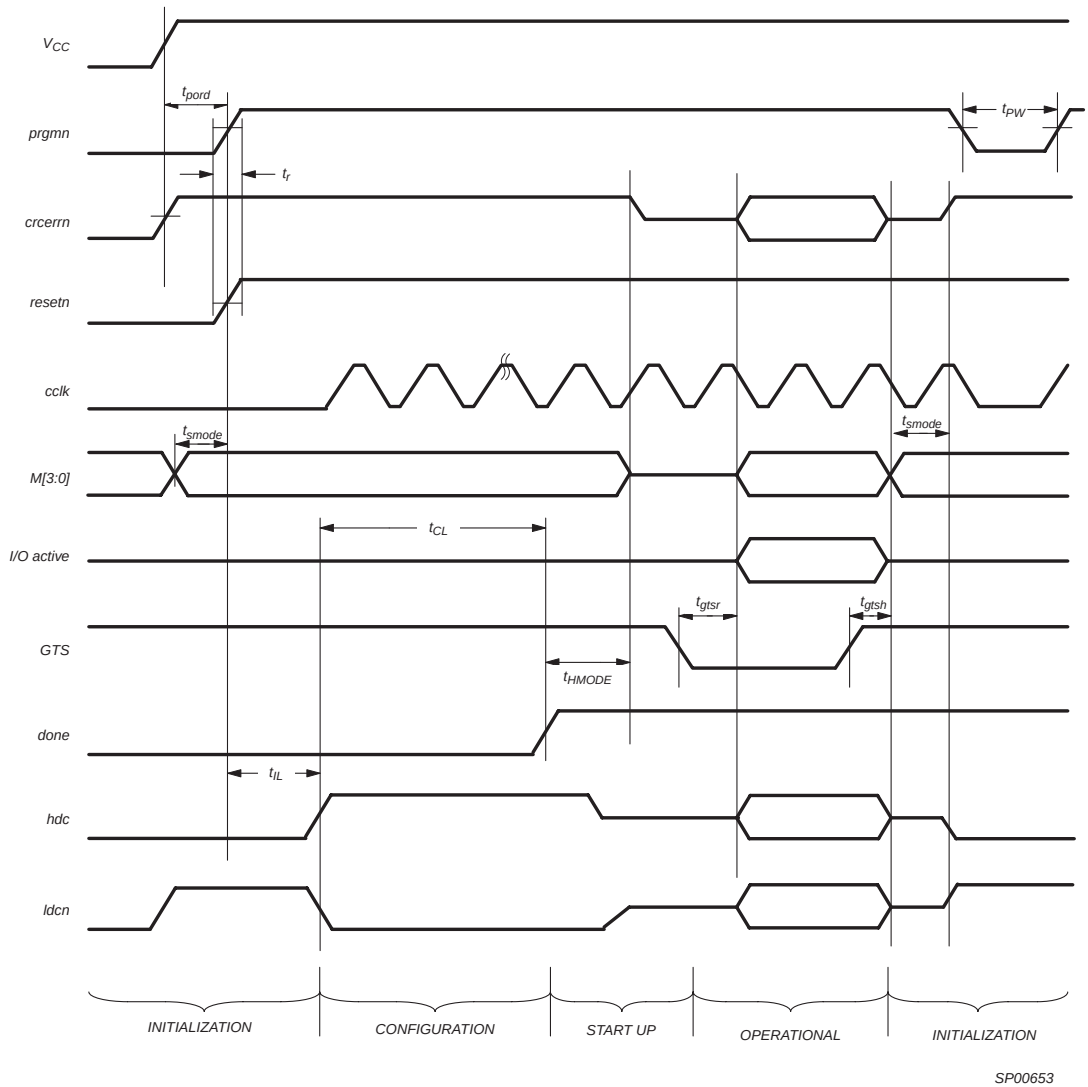


Figure 10: Using GTS Signal With Power-up to Avoid Signal Contention with Multi-function Pins Used as I/O

Configuration Data Format Overview

The XCR3960 functionality is determined by the state of internal configuration RAM. This section discusses the configuration data format, and the function of each field in configuration data packets.

Configuration Data Packets

Configuration of the XCR3960 is done using configuration packets. The configuration packet is shown in Figure 11. The configuration frame size is shown in Table 4. The data packet consists of a header and a data frame. There are four types of data frames. The header is shifted into the device first, followed by one data frame. Configuration of a single XCR3960 requires 1010 data packets, one for each address. All preceding data must contain only 1s. Once a device is configured, it retransmits data of any polarity. Before and during configuration, all data retransmitted out the daisy-chain port (DOUT) are 1s.

The ordering of the data packets may be random, and they cannot be mixed with other devices' data packets. Alignment bits are not required between data packets. If used, alignment bits must be included in the length count, and they must be at least two bits long.

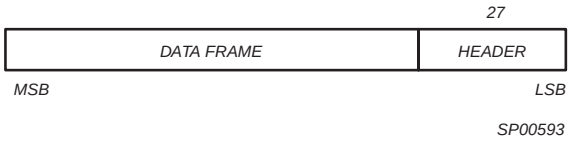


Figure 11: Data Packet

Table 4: Configuration Frame Size

Device	XCR3960
Number of frames	1010
Data bits/standard frame	560
Data bits/compressed frame	14
Data bits/user_code frame	560
Data bits/isc_code frame	560
Maximum configuration data – # bits/frame x # frames	565600

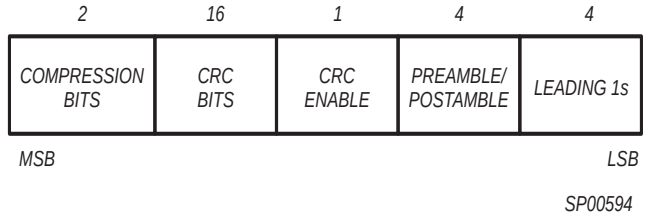


Figure 12: 27-bit Header

The header (Figure 12) is fixed and consists of five fields:

- Leading 1s
- Preamble
- CRC Enable
- CRC Bits
- Compression Bits

The leading 1s enter the device first. The following is a description of each field in the header.

Leading 1s:
This is a four or greater bit field consisting of 1s.

Preamble/Postamble:
This is a 4-bit field which indicates the start of a frame or the end of configuration:
Preamble: 0010 - signals the beginning of a configuration data packet
Postamble: 0100 - signals the end of configuration
All other values of the preamble field force configuration of the entire system to restart.

The segments CRC Enable, CRC Bits, and Compression Bits are valid only if the Preamble field is 0010.

Cyclic Redundancy Check (CRC) Enable:
In this single bit field, a "0" disables CRC checking of the data stream. If the CRC is disabled the 16-bit CRC field must be the default described below.
A1enables CRC error checking of the data stream.

CRC Error Checking:
The CRC field is a 16-bit field. The default value is 1010_1010_1010_1010. The calculated value is from data, address, stop bit, and first alignment bit (starting with crc_reg[15:0] = [0]). Using verilog operators, the CRC is calculated as:

```
crc_reg[14:2] <= cr_reg[14:2] << 1;
cr_reg[2] <= cr_reg[15]^din^cr_reg[1];
cr_reg[1] <= cr_reg[0];
cr_reg[0] < cr_reg[15]^din;
cr_reg[15] <= cr_reg[15]^din^cr_reg[14];
```

If a CRC error is detected, configuration is halted and must be restarted.

Compression Bits:

This 2-bit field defines the use of compression of the data packets.

00 - Standard mode:

The data packet contains both address and data.

01 - Reset mode:

The data packet contains only the address field. This pattern causes the configuration register to be reset.

10 - Hold mode:

The data packet contains only the address field. This pattern causes the configuration register to hold its value.

11 - Set mode:

The data packet contains only the address field. This pattern causes the configuration register to be set.

Data Frames

The four types of data frames are standard, compressed, user_code, and isc_code. All fields must be completely filled, with 1s used to fill unused bits. The definition of each frame is described below:

Standard Frame:

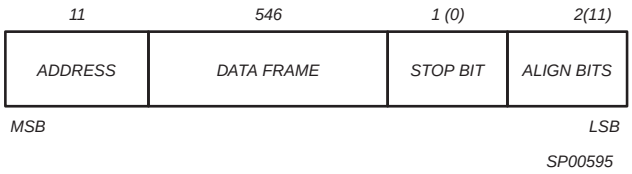


Figure 13: Standard Frame

Address:

This is an 11-bit filed for providing 1011 (1008 SRAM plus 3user) addresses.

Data:

546-bit field.

Stop bit:

This is a 1-bit field which must be 0.

Align bit:

This is a 2-bit field which must be 11.

Compressed Frame:

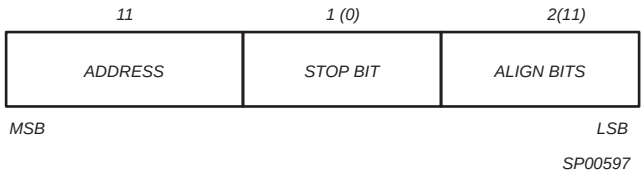


Figure 14: Compressed Frame

The compressed frame contains no data.

User Code Frame:

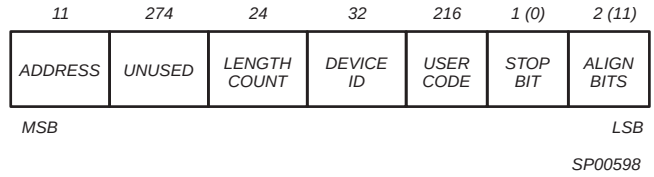


Figure 15: User Code Frame

The user code is located at address 1008D.

Length count:

This is a 24-bit field containing the length of the data-stream transmitted to configure all of the devices in the daisy chain. This field is only used by a XCR3960 if it is in the master mode.

Device ID:

This is a 32-bit field containing XCR3960 device ID:

492 SBGA:

0000_001_001_101000_1_000_00000010101_1

User Code:

This is a 216-bit field reserved for user information.

ISC Code Frame:

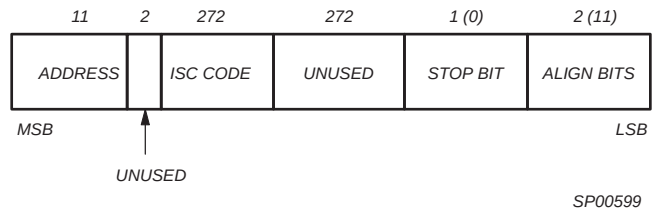


Figure 16: ISC Frame

The isc_code address is 1009.

The ISC frame allows the user to write an ISC code to the device.

Reconfiguration

To reconfigure the XCR3960 when the device is operating in the system, a low pulse is input into PRGMN. The I/Os not used for configuration are 3-stated. The XCR3960 then samples the mode select inputs and begins reconfiguration. The mode pins are continuously sampled, so the signals must be stable while PRGMN is Low. When configuration is compete, DONE is released, allowing it to be pulled High.

CRC Error Checking

CRC checking is done on each frame if enabled by setting the CRCerrn bit in the header. If there is an error, a CRC error is flagged by pulling CRCerrn Low. The XCR3960 is forced into the initialization state, and then moves into the configuration state after PRGMN and RESETN go High.

The XCR3960 will also pull CRCerrn Low if an invalid preamble is detected within a configuration data packet.

XCR3960 Configuration Modes

The method for configuring the XCR3960 is selected by the M0, M1, and M2 inputs. The M3 input should be High for all modes. In master modes, CCLK is an output with a nominal frequency of 1 MHz. In slave modes, CCLK is an input with a maximum frequency of 10 MHz if configuring only a single device, and 1 MHz if devices are daisy chained.

Master Serial Mode

In the master serial mode, the XCR3960 loads the configuration data from an external serial ROM. The configuration data is either loaded automatically at start-up or on a command to reconfigure. Xilinx Serial EEPROMs can be used to configure the XCR3960 in the master serial mode. This provides a simple 4-pin interface in an 8-pin package. Serial EEPROMs are available in 32K, 64K, 128K, 256K, and 1M-bit densities.

Configuration in the master serial mode can be done at power-up and/or upon a configure command. The system or the XCR3960 must activate the serial EEPROMs $\overline{\text{RESET}}$/OE and $\overline{\text{CE}}$ inputs. At power-up, the XCR3960 and serial EEPROM each contain internal power-on reset circuitry which allows the XCR3960 to be configured without the system providing an external signal. The power-on reset circuitry causes the serial EEPROMs' internal address pointer to be reset. After power-up, the XCR3960 automatically enters its initialization phase.

The serial EEPROM/XCR3960 interface used depends on such factors as the availability of a system reset pulse, availability of an intelligent host to generate a configure command, whether a single serial EEPROM is used or multiple serial ROMs are cascaded, whether the serial EEPROM contains a single or multiple configuration programs, etc.

Data is read into the XCR3960 sequentially from the serial ROM. The DATA output from the serial EEPROM is connected directly into the DIN input of the XCR3960. The CCLK output from the XCR3960 is connected to the CLOCK input of the serial EEPROM. During the configuration process, CCLK clocks one data bit into the XCR3960 on each rising edge.

Since the data and clock are direct connects, the XCR3960/serial EEPROM interface task is to use the system or XCR3960 to enable the $\overline{\text{RESET}}$/OE and $\overline{\text{CE}}$ of the serial EEPROM(s). The serial EEPROM's $\overline{\text{RESET}}$/OE is programmable to function with $\overline{\text{RESET}}$ active Low and OE active High, which allows HDC from the XCR3960 to control this function.

Likewise, the serial EEPROM could be programmed to function with RESET active High and $\overline{\text{OE}}$ active Low, allowing the LDCN pin from the XCR3960 to control this function. The XCR3960 done pin is connected to the serial EEPROM $\overline{\text{CE}}$ to enable the EEPROMs during configuration and disable them when configuration is complete.

In Figure 17, the serial EEPROMs $\overline{\text{RESET}}$/OE pin has been programmed to function with $\overline{\text{RESET}}$ active Low and OE active High, and it is controlled by the XCR3960's HDC pin. This resets the serial EEPROMs during the initialization state and enables their output during the configuration state. If a bit error is found during configuration, HDC will go Low, signifying the XCR3960 is back in initialization state and also resetting the EEPROMs. This restarts the configuration process.

The XCR3960 DONE pin is routed to the $\overline{\text{CE}}$ pin of the EEPROMs. The Low signal on DONE during configuration enables the serial EEPROMs. At the completion of configuration, the High on DONE disables the EEPROMs.

In Figure 17, three serial EEPROMs are cascaded to configure a XCR3960. When configuration data requirements exceed the capacity of a single serial EEPROM, multiple serial EEPROMs can be cascaded to support the configuration of a single (or multiple) XCR3960(s). After the last bit from the first serial ROM is read, the serial ROM outputs $\overline{\text{CEO}}$ Low and 3-states the DATA output. The next serial ROM recognizes the Low on $\overline{\text{CE}}$ input and outputs configuration data on the DATA output. After configuration is complete, the XCR3960's done output into $\overline{\text{CE}}$ disables the serial EEPROMs.

In applications in which a serial EEPROM stores multiple configuration programs, the subsequent configuration program(s) are stored in EEPROM locations that follow the last address for the previous configuration program. The user must ensure that the serial EEPROMs address pointer is not reset, causing the first device configuration to be reloaded.

Contention on the XCR3960s DIN pin must be avoided. During configuration, DIN receives configuration data. After configuration, it is a user I/O.

Figure 18 shows the master serial configuration mode timing diagram, and Table 5 the master serial configuratoin mode timing characteristics.

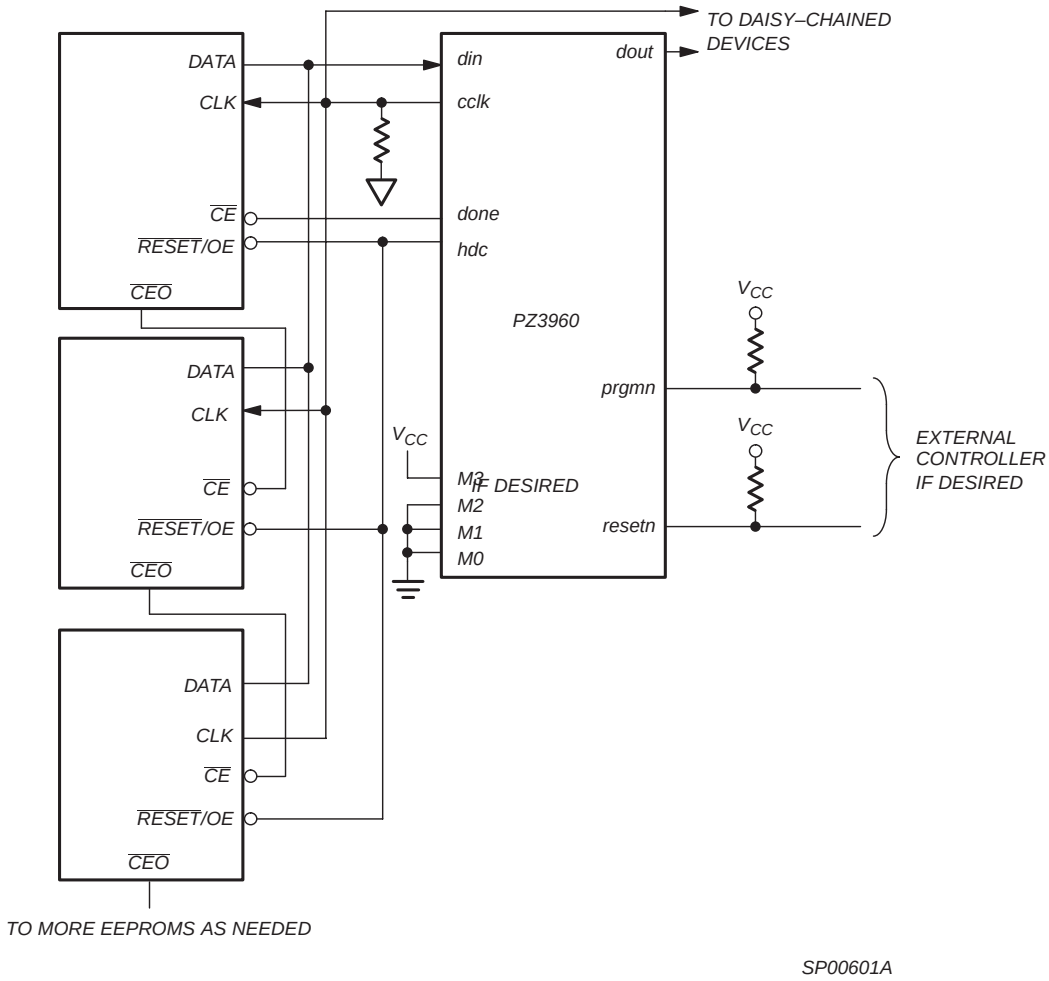


Figure 17: Master Serial Configuration

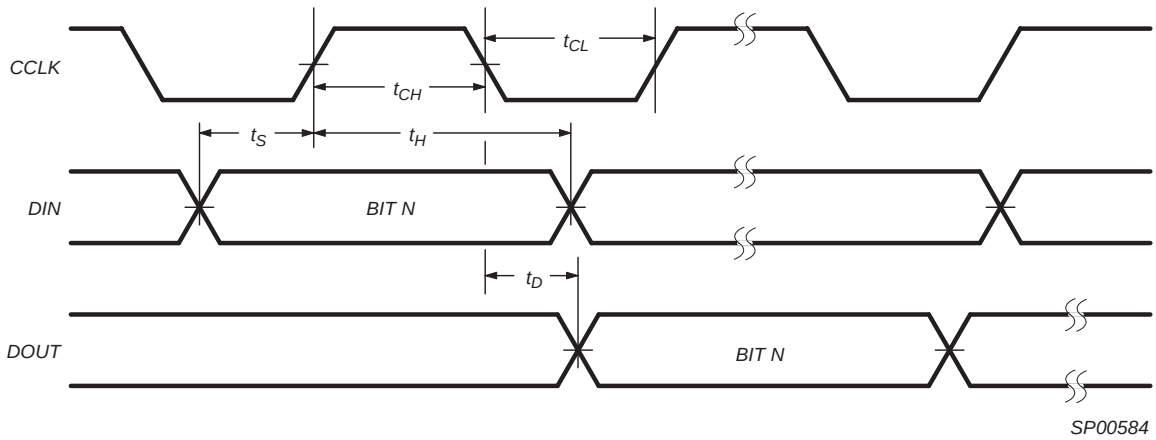


Figure 18: Master Serial Configuration Mode Timing Diagram

Table 5: Master Serial Configuration Mode Timing Characteristics

Symbol	Parameter		Min	Nom	Max	Unit
t_S	DIN setup time		60			ns
t_H	DIN hold time		0			ns
t_D	CCLK to DOUT delay				300	ns
t_{CL}	CCLK Low time	M3 = 1	357	500	833	ns
t_{CH}	CCLK High time	M3 = 1	357	500	833	ns
t_C	CCLK frequency	M3 = 1	0.6	1.0	1.4	MHz

Master Parallel Mode

The master parallel configuration mode is generally used to interface to industry-standard byte-wide memory such as 256K and larger EEPROMs. Figure 19 provides the interface for master parallel mode. The XCR3960 outputs a 20-bit address on A[19:0] to memory and reads one byte of configuration data every eighth CCLK. The parallel bytes are internally serialized starting with the least significant bit, D0. The starting memory address is 00000 Hex and the XCR3960 increments the address for each byte loaded. The starting address is output when the device enters the configuration state. The XCR3960 latches the data byte on the second rising edge of CCLK. This next data byte is latched in the XCR3960 seven CCLK cycles later.

Figure 19 shows the master parallel configuration timing diagram, and Table 6 the master parallel configuration mode timing characteristics.

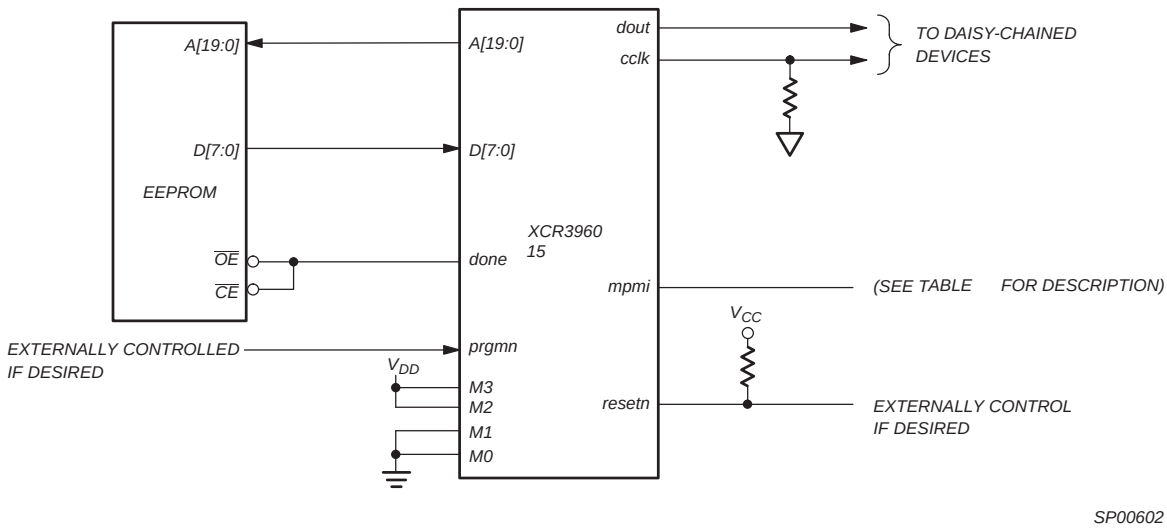


Figure 19: Master Parallel Configuration

Table 6: Master Parallel Configuration Mode Timing Characteristics

Symbol	Parameter		Min	Nom	Max	Unit
t_{AV}	CCLK to address valid		0		200	ns
t_S	D[7:0] setup time to CCLK High		60			ns
t_H	D[7:0] hold time from CCLK High		0			ns
t_{CL}	CCLK Low time	M3 = 1	357	500	833	ns
t_{CH}	CCLK High time	M3 = 1	357	500	833	ns
t_D	CCLK to DOUT delay				300	ns
f_C	CCLK frequency	M3 = 1	0.6	1.0	1.4	MHz

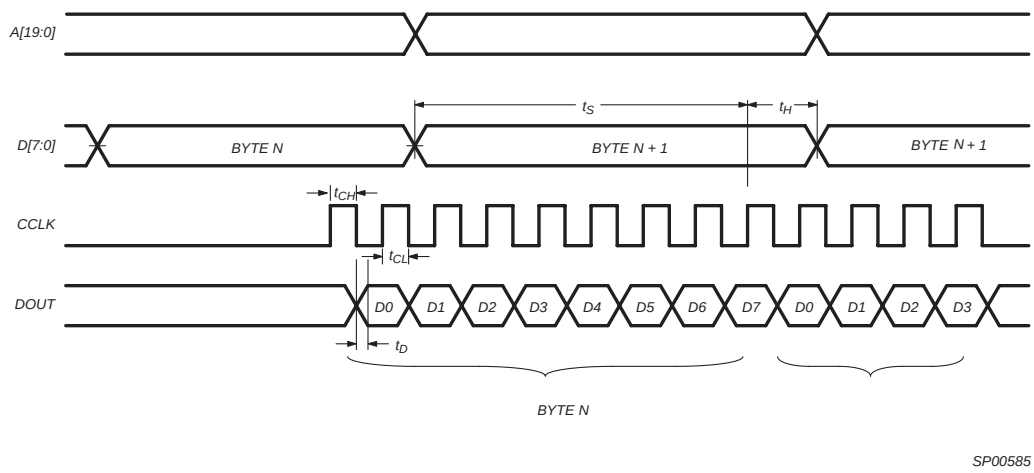


Figure 20: Master Parallel Configuration Mode Timing Diagram

Synchronous Peripheral Mode

In the synchronous peripheral mode, byte-wide data is input into D[7:0] on the rising edge of the CCLK input. The first data byte is clocked in on the second CCLK after HDC goes high. Subsequent data bytes are clocked in on every eighth rising edge of CCLK. The process repeats until all of the data is loaded into the XCR3960. The serial data begins shifting out on DOUT 0.5 cycles after the parallel data was loaded. It requires additional cclks after the last byte is loaded to complete the shifting. Figure 21 shows the interface for synchronous peripheral mode. When configuring a single device, the frequency of CCLK can be up to 10 MHz. As with master modes, this mode can be used for the lead XCR3960 for daisy-chained devices. Note that the CCLK frequency for daisy-chained operation is limited to 1 MHz. Figure 22 shows the synchronous periphal configuratoin mode timing diagram, and Table 7 the synchronous peripheral configuration mode timing characteristics.

Also note that CS1 is a multi-function pin, which means that it is available as a user I/O during normal device operation. As with all user I/O on the XCR3960, CS1 has an internal pull-down resistor that is automatically activated if the I/O pin is not used (see section on terminations for more information). If CS1 is left attached to V_{CC} after configuration, and it is not used as an I/O, the internal pull-down must be disabled or a path from V_{CC} to ground is created. To disable the pull-down, use the XPLA property statement '*signal name:pin number* tri-state' to disable the resistor.

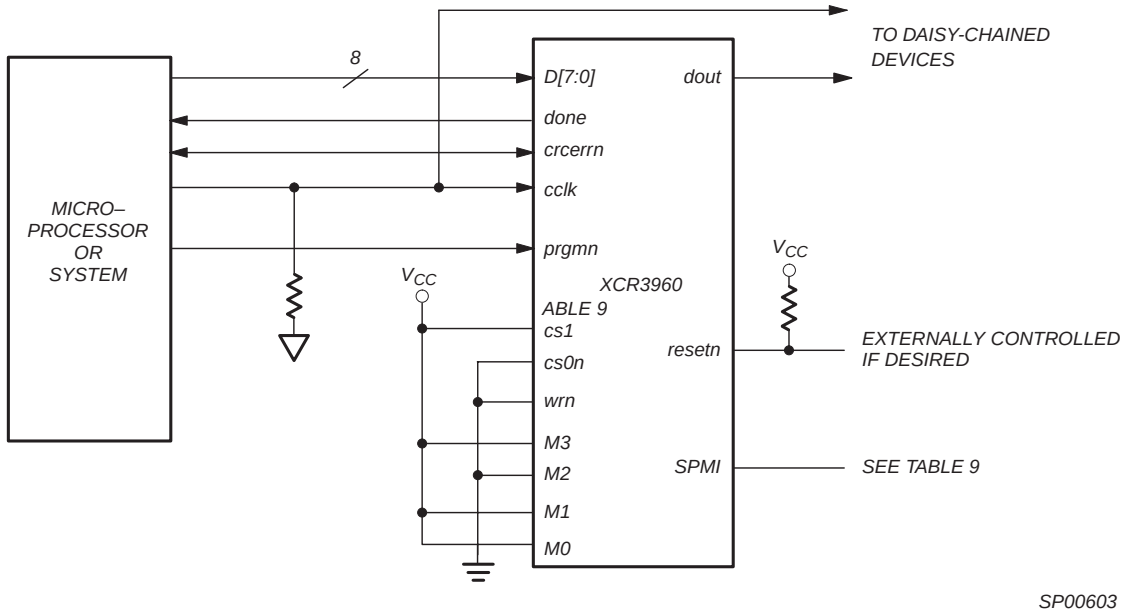


Figure 21: Synchronous Peripheral Configuration

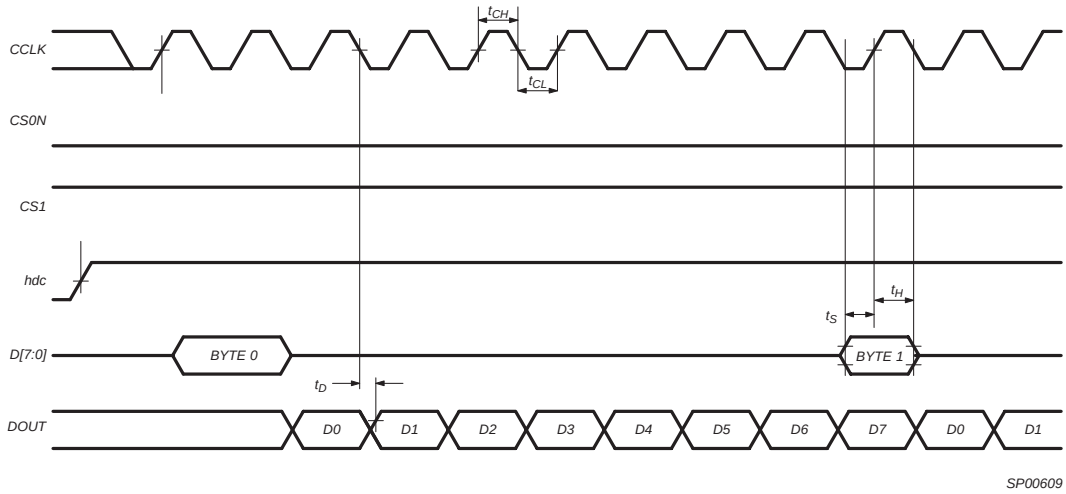


Figure 22: Synchronous Peripheral Configuration Mode Timing Diagram

Table 7: Synchronous Peripheral Configuration Mode Timing Characteristics

Symbol	Parameter		Min	Max	Unit
t_S	D[7:0] setup time		20	0	ns
t_H	D[7:0] hold time		0		ns
t_{CH}	CCLK High time	Single device	50		ns
		Daisy-chain device	500		ns
t_{CL}	CCLK Low time	Single device	50		ns
		Daisy-chain device	500		ns
f_C	CCLK frequency	Single device		10	MHz
		Daisy-chain device		1	MHz

Slave Serial Mode

Figure 23 shows the interface for the slave serial configuration mode. The configuration data is provided into the XCR3960s DIN input synchronous with the CCLK input. After the XCR3960 has loaded its configuration data, it retransmits incoming configuration data on DOUT. When configuring a single device, the frequency of CCLK can be up to 10 MHz. Figure 23 shows the slave serial configuration mode timing diagram, and Table 8 the slave serial configuration mode timing characteristics.

A device in slave serial mode can be used as the lead device in a daisy chain. When used in daisy-chained operation, CCLK is routed into all slave serial mode devices in parallel and the frequency is limited to 1 MHz. The DOUT pin of the lead device is connected to the DIN pin of the next device, and so on. In daisy-chained operation, all downstream devices use slave serial mode regardless of the configuration mode of the lead device.

Multiple slave XCR3960s can be loaded with identical configurations simultaneously. This is done by loading the configuration data into the din inputs in parallel.

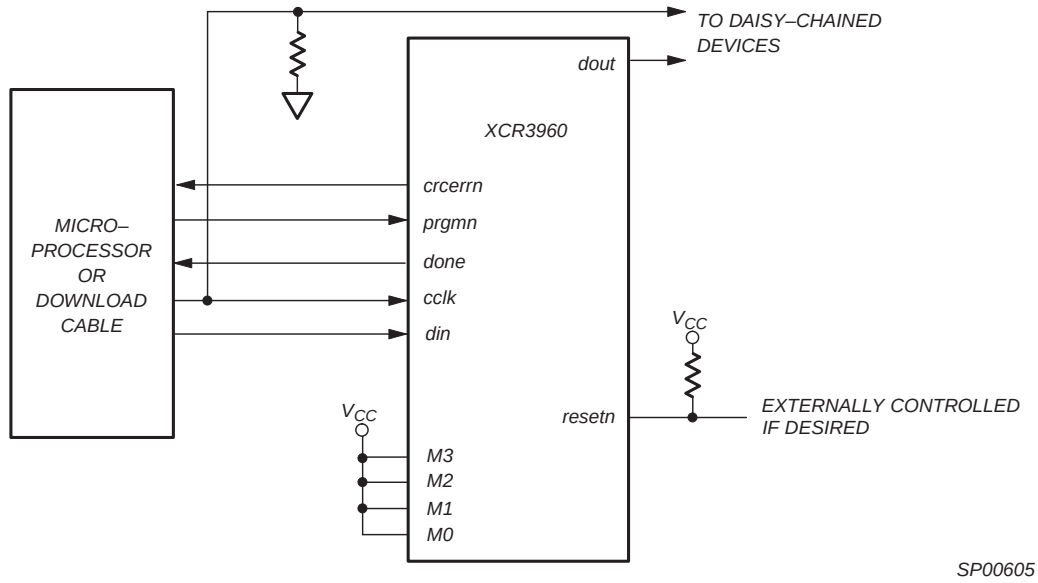


Figure 23: Slave Serial Configuration Schematic

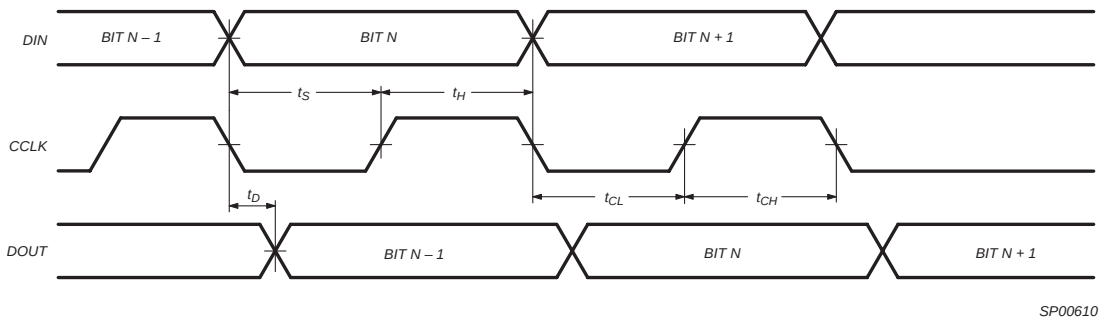


Figure 24: Slave Serial Configuration Mode Timing Diagram

Table 8: Slave Serial Configuration Mode Timing Characteristics

Symbol	Parameter		Min	Max	Unit
t_S	DIN setup time		20	0	ns
t_H	DIN hold time		0		ns
t_{CH}	CCLK High time	Single device	50		ns
		Daisy-chain device	500		ns
t_{CL}	CCLK Low time	Single device	50		ns
		Daisy-chain device	500		ns
f_C	CCLK frequency	Single device		10	MHz
		Daisy-chain device		1	MHz

Slave Parallel Mode

The slave parallel mode is essentially the same as the synchronous peripheral mode, except that the chip select pins (CS1 and CS0n) are not used. As in the synchronous peripheral mode, byte-wide data is input into D[7:0] on the rising edge of the CCLK input. The first data byte is clocked in on the second CCLK after HDC goes High. Subsequent data bytes are clocked in on every eighth rising edge of CCLK. The process repeats until all of the data is loaded into the XCR3960. The serial data begins shifting out on DOUT 0.5 cycles after the parallel data was loaded. It requires additional CCLKs after the last byte is loaded to complete the shifting. Figure 25 shows the interface for slave parallel mode. When configuring a single device, the frequency of CCLK can be up to 10 MHz. Figure 26 shows the slave parallel configuration mode timing diagram, and Table 9 the slave parallel configuration mode timing characteristics.

As with synchronous peripheral mode, the slave parallel mode can be used as the lead XCR3960 for daisy-chained devices. Note that the CCLK frequency for daisy-chain operation is limited to 1 MHz.

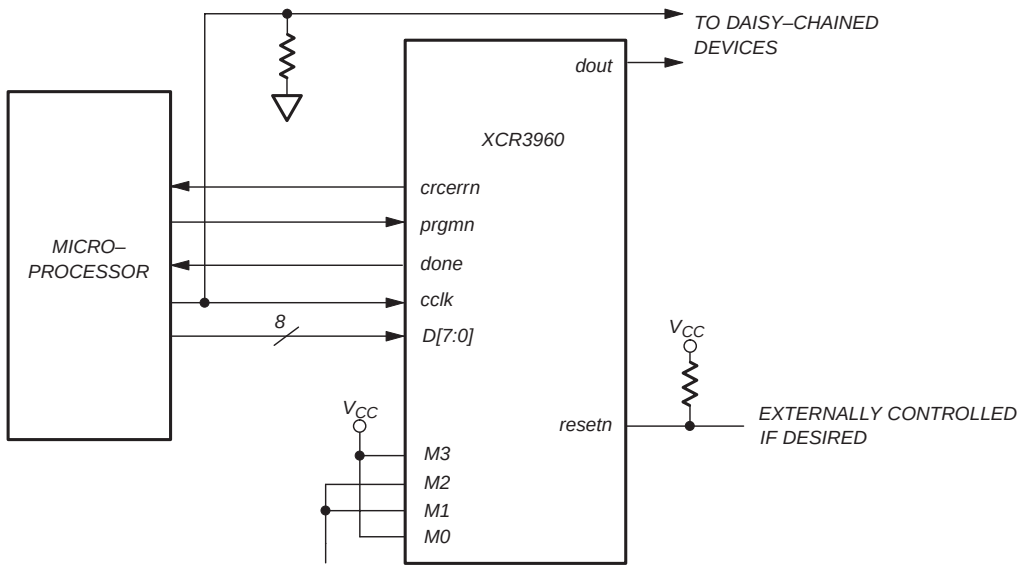


Figure 25: Slave Parallel Configuration Schematic

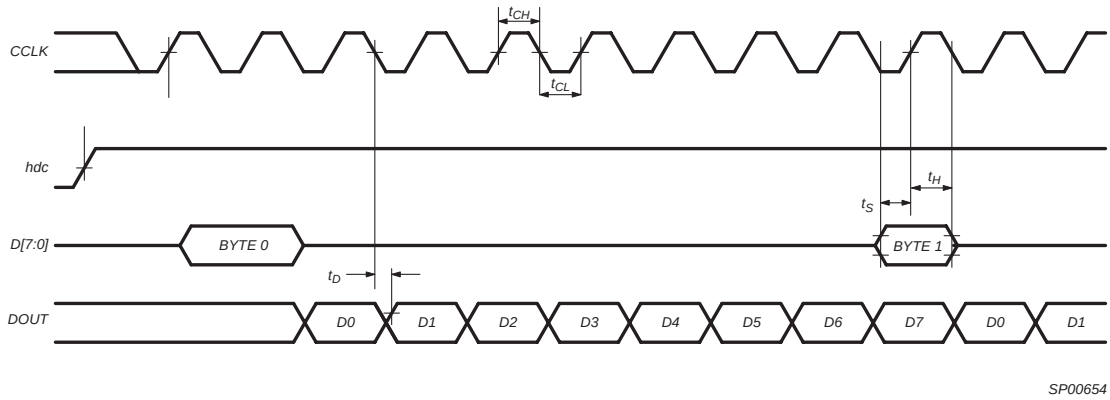


Figure 26: Slave Parallel Configuration Mode Timing Diagram

Table 9: Slave Parallel Configuration Mode Timing Characteristics

Symbol	Parameter		Min	Max	Unit
t_S	D[7:0] setup time		20	0	ns
t_H	D[7:0] hold time		0		ns
t_{CH}	CCLK High time	Single device	50		ns
		Daisy-chain device	500		ns
t_{CL}	CCLK Low time	Single device	50		ns
		Daisy-chain device	500		ns
f_C	CCLK frequency	Single device		10	MHz
		Daisy-chain device		1	MHz

Daisy-Chain Operation

Multiple XCR3960s can be configured by using a daisy-chain of XCR3960s. Daisy-chaining uses a lead XCR3960 and one or more XCR3960s configured in slave serial mode. The lead XCR3960 can be configured in any mode. Figure 27 shows the connections for loading multiple XCR3960s in a daisy-chain configuration with the lead devices configured in master parallel mode. Figure 28 shows the connections for loading multiple XCR3960s with the lead device configured in master serial mode.

Daisy-chained XCR3960s are connected in series. An upstream XCR3960 which has received the preamble outputs a high on DOUT, ensuring that downstream XCR3960s do not receive frame start bits. When the lead device receives the postamble, its configuration is complete. At this point, the configuration RAM of the lead device is full and its DONE pin is released. The lead device continues to load configuration data until the internal frame bit counter reaches the length count or all the DONE pins of the chain have gone High. Since the configuration RAM of the lead device is full, this data is shifted out serially to the downstream devices on the DOUT pin. As the configuration is completed for the downstream devices, each will release its DONE pin. Because the DONE pins of each device in the chain are wire-anded together, the DONE pin will be pulled High when all devices in the daisy-chain have completed configuration. All devices now move to the start-up state simultaneously.

The generation of CCLK for the daisy-chained devices which are in slave serial mode differs depending on the configuration mode of the lead device. A master parallel mode device uses its internal timing generator to produce an internal CCLK. If the lead device is configured in either synchronous peripheral, slave serial mode, or slave parallel mode, CCLK is an input and is mated to the lead device and to all of the daisy-chained devices in parallel. The configuration data is read into DIN of slave devices on the positive edge of CCLK, and shifted out DOUT on the negative edge of CCLK. Note that daisy-chain operation is limited to a CCLK frequency of 1 MHz. If a CRC error or an invalid preamble is detected by a slave device, CRCerrn will be pulled Low and in turn pull PRGMN Low, halting configuration for all devices. If a CRC error is detected by the master device, HDC will be pulled Low, resetting the EEPROM to the first address and restarting configuration.

The development software can create a composite configuration file for configuring daisy-chained XCR3960s. The configuration data consists of multiple concatenated data packets.

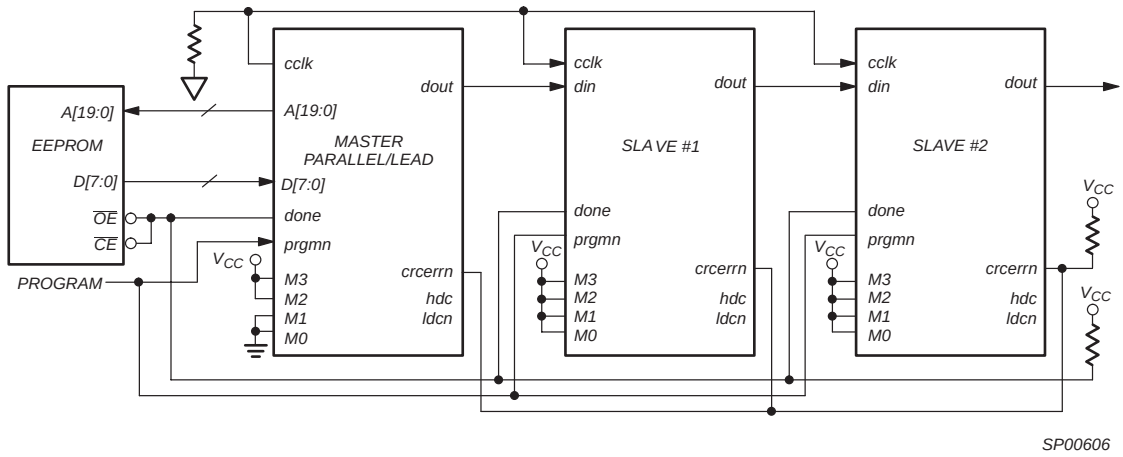


Figure 27: Daisy-chain Schematic with Lead Device in Master Parallel

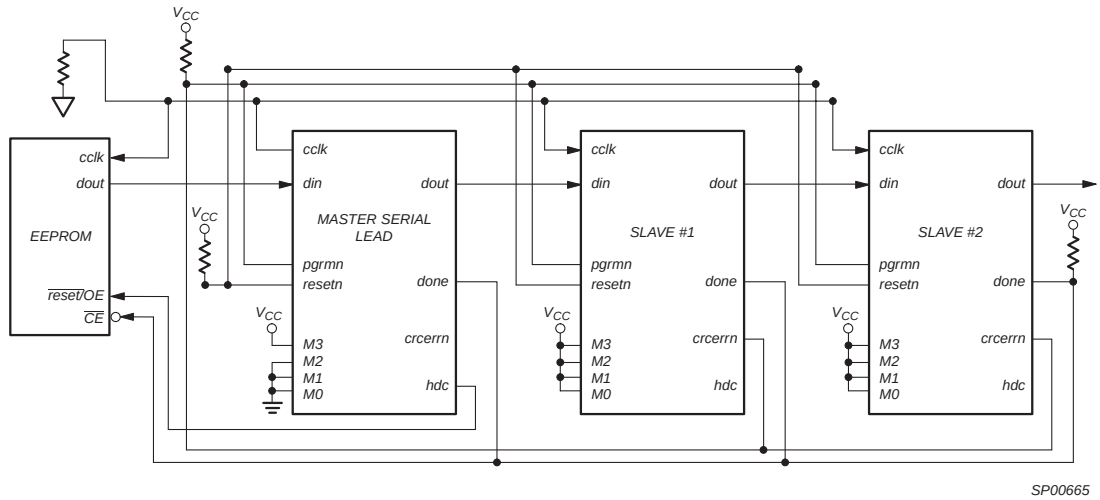


Figure 28: Daisy-chain Schematic with Master Serial Lead Device

JTAG Testing Capability

JTAG is the commonly-used acronym for the Boundary Scan Test (BST) feature defined for integrated circuits by IEEE Standard 1149.1. This standard defines input/output pins, logic control functions, and commands which facilitate both board and device level testing without the use of specialized test equipment. BST provides the ability to test the external connections of a device, test the internal logic of the device, and capture data from the device during normal operation. BST provides a number of benefits in each of the following areas:

- Testability
  - Allows testing of an unlimited number of interconnects on the printed circuit board
  - Testability is designed in at the component level
    - Enables desired signal levels to be set at specific pins (Preload)
    - Data from pin or core logic signals can be examined during normal operation
- Reliability
  - Eliminates physical contacts common to existing test fixtures (e.g., "bed-of-nails")
  - Degradation of test equipment is no longer a concern
  - Facilitates the handling of smaller, surface-mount components
  - Allows for testing when components exist on both sides of the printed circuit board
- Cost
  - Reduces/eliminates the need for expensive test equipment

- Reduces test preparation time
- Reduces spare board inventories

The Xilinx XCR3960s JTAG interface includes a TAP Port and a TAP Controller, both of which are defined by the IEEE 1149.1 JTAG Specification. As implemented in the Xilinx XCR3960, the TAP Port includes five pins (refer to Table 10) described in the JTAG specification: TCK, TMS, TDI, TDO, and TRSTN. These pins should be connected to an external pull-up resistor to keep the JTAG signals from floating when they are not being used.

Table 11 defines the dedicated pins used by the mandatory JTAG signals for the XCR3960.

The JTAG specifications define two sets of commands to support boundary-scan testing: high-level commands and low-level commands. High-level commands are executed via board test software on an a user test station such as automated test equipment, a PC, or an engineering workstation (EWS). Each high-level command comprises a sequence of low level commands. These low-level commands are executed within the component under test, and therefore must be implemented as part of the TAP Controller design. The set of low-level boundary-scan commands implemented in the XCR3960 is defined in Table 12. By supporting this set of low-level commands, the XCR3960 allows execution of all high-level boundary-scan commands.

See Table 13 for the boundary scan timing characteristics.

Table 10: JTAG Pin Description

Pin	Name	Description
t_{CK}	Test Clock Output	Clock pin to shift the serial data and instructions in and out of the TDI and TDO pins, respectively. TCK is also used to clock the TAP Controller state machine.
t_{MS}	Test Mode Select	Serial input pin selects the JTAG instruction mode. TMS should be driven High during user mode operation.
t_{DI}	Test Data Input	Serial input pin for instructions and test data. Data is shifted in on the rising edge of TCK.
t_{DO}	Test Data Output	Serial output pin for instructions and test data. Data is shifted out on the falling edge of TCK. The signal is 3-stated if data is not being shifted out of the device.
t_{RSTN}	Test Reset	Forces TAP controller to test logic reset state. This signal is active Low.

Table 11: XCR3960 JTAG Pinout by Package Type

Device	(Pin Number / Macrocell #)				
XCR3960	t_{CK}	t_{MS}	t_{DI}	t_{DO}	t_{RSTN}
492-pin PBGA	P4	N4	P1	P3	N3

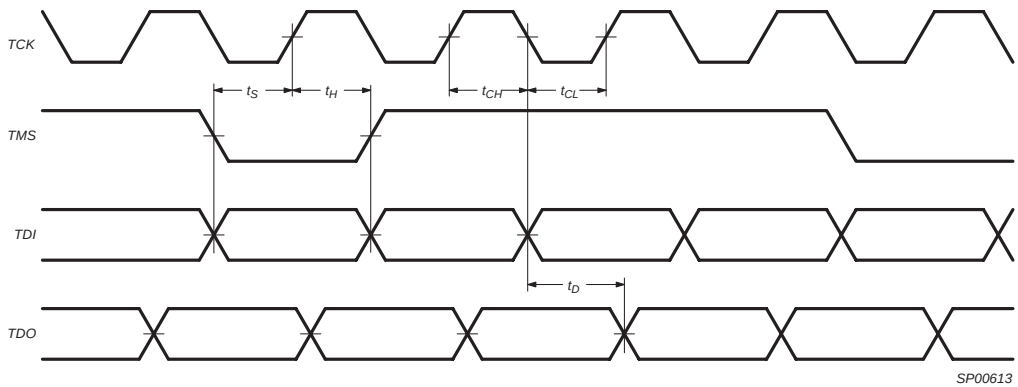


Figure 29: Boundary Scan Timing Diagram

Table 12: XCR3960 Low-Level JTAG Boundary-Scan Commands

Instruction (Instruction Code) Register Used	Description
SAMPLE/PRELOAD (00010) Boundary-Scan Register	The mandatory SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the boundary-scan shift-rRegister prior to selection of the other boundary-scan test instructions.
EXTEST (00000) Boundary-Scan Register	The mandatory EXTEST instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of boundary-scan shift-register using the SAMPLE/PRELOAD instruction prior to selection of the EXTEST instruction.
BYPASS (11111) Bypass Register	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. The BYPASS instruction can be entered by holding TDI at a constant high value and completing an Instruction-Scan cycle.
IDCODE (00001) Boundary-Scan Register	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. The IDCODE instruction permits blind interrogation of the components assembled onto a printed circuit board. Thus, in circumstances where the component population may vary, it is possible to determine what components exist in a product.
HIGHZ (00101) Bypass Register	The HIGHZ instruction places the component in a state in which all of its system logic outputs are placed in an inactive drive state (e.g., high-impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component. The HIGHZ instruction also forces the Bypass Register between TDI and TDO.
INTEST (00011) Boundary-Scan Register	The INTEST instruction allows testing of the on-chip system logic while the component is assembled on the board. The boundary-scan register is connected between TDI and TDO. Using the INTEST instruction, test stimuli are shifted in one at a time and applied to the on-chip system logic. The test results are captured into the boundary-scan register and are examined by subsequent shifting, Data would typically be loaded onto the latched parallel outputs of boundary-scan shift-register stages using the SAMPLE/PRELOAD instruction prior to selection of the INTEST instruction.

Note: Following use of the INTEST instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return or normal (i.e., nontest) operation.

Device Configuration Through JTAG

In addition to the normal configuration modes, the XCR3960 can also be configured through the JTAG port. This feature is very useful for design prototyping and debug before the device is put into the final product. In System Configuration of the XCR3960 is supported by Xilinx PC-ISP software. Table 14 shows the ISC commands supported by the XCR3960, and Table 15 details the AC and DC specifications for configuring the device through the JTAG port.

To configure the device through the JTAG port, mode pins M0, M1, and M2 should all be held Low. M3, as always, should be High and the JTAG pins should be terminated as described in "Terminations" on page 8 of this data sheet.

Table 13: Boundary Scan Timing Characteristics

Symbol	Parameter	Min	Max	Unit
t_S	TDI/TMS to TCK setup time	20		ns
t_H	TDI/TMS from TCK hold time	0		ns
t_{CH}	TCK High time	50		ns
t_{CL}	TCK Low time	50		ns
f_{TCK}	TCK frequency		10	MHz
t_D	TCK to TDO delay		35	ns

Table 14: Low Level ISP Commands

Instruction (Register Used)	Instruction Code	Description
Enable (ISP Shift Register)	1001	Enables the Erase and Program commands. Using the ENABLE instruction before the Erase and Program instructions allows the user to specify the outputs the device using the JTAG boundary-scan SAMPLE/PRELOAD command.
Erase (ISP Shift Register)	1010	Erases the entire EEPROM array. The outputs during this operation can be defined by user by using the JTAG SAMPLE/PRELOAD command.
Program (ISP Shift Register)	1011	Programs the data in the ISP Shift Register into the addressed EEPROM row. The outputs during this operation can be defined by user by using the JTAG SAMPLE/PRELOAD command.

Absolute Maximum Ratings(1)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	–0.5	4.6	V
V_{IN}	Input voltage	–1.2	V_{CC} + 0.5	V
V_{OUT}	Output voltage	–0.5	V_{CC} + 0.5	V
I_{IN}	Input current	–30	30	mA
T_J	Junction temperature range	–40	150	°C
T_{STG}	Storage temperature range	–65	150	°C

NOTE 1: Stresses above these listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.

Operating Range

Product Grade	Temperature	Voltage
Commercial	0 to 70°C	3.3V ±10%
Industrial	–40 to 85°C	3.3V ±10%

DC Electrical Characteristics For Commercial Grade Devices

Commercial temperature range: V_{CC} = 3.0V to 3.6V; 0°C < T_{AMB} < 70°C.

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{IH}	Input High voltage	V_{CC} = 3.6V	2.0	V_{CC} + 0.3	V
V_{IL}	Input Low voltage	V_{CC} = 3.0V	–0.3	0.8	V
V_{OH}	Output High voltage	V_{CC} = 3.0V I_{OH} = –8 mA	2.4		V
V_{OL}	Output Low voltage	V_{CC} = 3.0V I_{OH} = 8 mA		0.4	V
I_I	Input leakage current	V_{CC} = 3.6V 0 < V_{IN} < V_{CC}	–10	10	µA
I_{CCSB}	Standby current	T_{AMB} = 25°C; no output loads, inputs at V_{CC} or GND		100	µA
C_{IN}(1)	Input capacitance	T_{AMB} = 25°C; V_{CC} = 3.3V; f = 1 MHz		10	pF
C_{IO}(1)	I/O capacitance	T_{AMB} = 25°C; V_{CC} = 3.3V; f = 1 MHz		10	pF
C_{CLK}(1)	Clock pin capacitance	T_{AMB} = 25°C; V_{CC} = 3.3V; f = 1 MHz		12	pF
R_{DONE}(1)	DONE pull-up resistor	V_{CC} = 3.0V; V_{IN} = 0V	10	30	kΩ
R_{PD}(1)	Unused I/O pull-down resistor	V_{CC} = 3.6V; V_{IN} = V_{CC}	100	400	kΩ
I_{OZH}	Input leakage	V_{IN} = 3.6V	–10	10	µA
I_{OZL}	Input leakage	V_{IN} = 0.0V	–10	10	µA

Note 1: This parameter is guaranteed by design and characterization, not by test.

AC Electrical Characteristics for Commercial Devices

Commercial temperature range: V_{CC} = 3.0V to 3.6V; 0°C < T_{AMB} < 70°C.

Symbol	Parameter	Min	Max	Unit
Timing Requirements				
t_{CL}(1)	Clock Low time	2.5		ns
t_{CH}(1)	Clock High time	2.5		ns
t_{SU_PAL}	PAL setup time (Global clock)	4.0		ns
t_{SU_PLA}(1)	PLA setup time (Global clock)	5.5		ns
t_{SU_XOR}(1)	XOR setup time (Global clock)	6.5		ns
t_{H}(1)	Hold time (Global clock)		0	ns
Output Characteristics(2)				
t_{PD_PAL}	Input to output delay through PAL		7.5	ns
t_{PD_PLA}(1)	Input to output delay through PLA		9.0	ns
t_{PD_XOR}(1)	Input to output delay through $\overline{\text{XOR}}$		10.0	ns
t_{PDF_PAL}(1)	Input (or feedback-node) to internal feedback-node delay time through PAL		4.0	ns
t_{PDF_PLA}(1)	Input (or feedback-node) to internal feedback-node delay time through PLA		5.5	ns
t_{PDF_XOR}(1)	Input (or feedback-node) to internal feedback-node delay time through XOR		6.5	ns
t_{CF}(1)	Global clock to feedback delay		2.5	ns
t_{CO}	Global clock to out delay		6.0	ns
t_{CS}(1)	Clock skew (variance for switching outputs with common global clock)		1.0	ns
f_{MAX1}(1)	Maximum flip-flop toggle rate $\left(\frac{1}{t_{CL} + t_{CH}}\right)$	200		MHz
f_{MAX2}(1)	Maximum internal frequency $\left(\frac{1}{t_{SU-PAL} + t_{CO}}\right)$	154		MHz
f_{MAX3}(1)	Maximum external frequency $\left(\frac{1}{t_{SU-PAL} + t_{CO}}\right)$	100		MHz
t_{BUFF}(1)	Output buffer delay (fast)		3.5	ns
t_{SSR}(1)	Slow slew rate incremental delay		8.0	ns
t_{EA}(1)	Output enable delay		8.0	ns
t_{ER}(1)	Output disable delay		8.0	ns
t_{GTSA}(1)	Global 3-state enable		40.0	ns
t_{GTSR}(1)	Global 3-state disable		40.0	ns
t_{RR}(1)	Input to register reset		10.5	ns
t_{RP}(1)	Input to register preset		10.5	ns
t_{GRR}(1)	Global reset to register reset		40	ns
t_{GZIA}(1)	Global ZIA delay		4.0	ns

Note 1: This parameter is guaranteed by design and characterization, not by test.
Note 2: Output C_L = 5.0 pF.

DC Electrical Characteristics For Industrial Grade Devices

Industrial temperature range: V_{CC} = 3.0V to 3.6V; –40°C < T_{AMB} < 850°C.

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{IH}	Input High voltage	V_{CC} = 3.6V	2.0	V_{CC} + 0.3	V
V_{IL}	Input Low voltage	V_{CC} = 3.0V	–0.3	0.8	V
V_{OH}	Output High voltage	V_{CC} = 3.0V; I_{OH} = –8 mA	2.4		V
V_{OL}	Output Low voltage	V_{CC} = 3.0V; I_{OH} = 8 mA		0.4	V
I_I	Input leakage current	V_{CC} = 3.6V; 0 < V_{IN} < V_{CC}	–10	10	µA
I_{CCSB}	Standby current	T_{AMB} = 25°C; No output loads, Inputs at V_{CC} or GND.		100	µA
C_{IN}(2)	Input capacitance	T_{AMB} = 25°C; V_{CC} = 3.3V; f = 1 MHz		10	pF
C_{IO}(2)	I/O capacitance	T_{AMBb} = 25°C; V_{CC} = 3.3V; f = 1 MHz		10	pF
C_{CLK}(2)	Clock pin capacitance	T_{AMB} = 25°C; V_{CC} = 3.3V; f = 1 MHz		12	pF
R_{DONE}(2)	DONE pull-up resistor	V_{CC} = 3.0V; V_{IN} = 0V	10	30	kΩ
R_{PD}(2)	Unused I/O pull-down resistor	V_{CC} = 3.6V; V_{IN} = V_{CC}	100	400	kΩ
I_{OZH}	Input leakage	V_{IN} = 3.6V	–10	10	µA
I_{OZL}	Input leakage	V_{IN} = 0.0V	–10	10	µA

Note 1: This parameter is guaranteed by design and characterization, not by test.

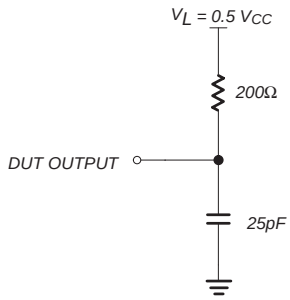
AC Electrical Characteristics For Industrial Grade Devices

Industrial temperature range: V_{CC} = 3.0V to 3.6V; –40°C < T_{AMB} < 85°C.

Symbol	Parameter	Min	Max	Unit
Timing Requirements				
t_{CL}(1)	Clock Low time	2.5		ns
t_{CH}(1)	Clock High time	2.5		ns
t_{SU_PAL}	PAL setup time (Global clock)	4.5		ns
t_{SU_PLA}(1)	PLA setup time (Global clock)	6.0		ns
t_{SU_XOR}(1)	XOR setup time (Global clock)	7.0		ns
t_{H}(1)	Hold time (Global clock)		0	ns
Output Characteristics(2)				
t_{PD_PAL}(1)	Input to output delay through PAL		8.0	ns
t_{PD_PLA}(1)	Input to output delay through PLA		9.5	ns
t_{PD_XOR}(1)	Input to output delay through XOR		10.5	ns
t_{PDF_PAL}(1)	Input (or feedback node) to internal feedback node delay time through PAL		4.0	ns
t_{PDF_PLA}(1)	Input (or feedback node) to internal feedback node delay time through PLA		5.5	ns
t_{PDF_XOR}(1)	Input (or feedback node) to internal feedback node delay time through XOR		6.5	ns
t_{CF}(1)	Global clock to feedback delay		2.5	ns
t_{CO}(1)	Global clock to out delay		6.5	ns
t_{CS}(1)	Clock skew (variance for switching outputs with common global clock)		1.0	ns
f_{MAX1}(1)	Maximum flip-flop toggle rate $\left(\frac{1}{t_{CL} + t_{CH}}\right)$	200		MHz
f_{MAX2}(1)	Maximum internal frequency $\left(\frac{1}{t_{SU-PAL} + t_{CO}}\right)$	143		MHz
f_{MAX3}(1)	Maximum external frequency $\left(\frac{1}{t_{SU-PAL} + t_{CO}}\right)$	91		MHz
t_{BUFF}(1)	Output buffer delay (fast)		4.0	ns
t_{SSR}(1)	Slow slew rate incremental delay		8.0	ns
t_{EA}(1)	Output enable delay		8.5	ns
t_{ER}(1)	Output disable delay[1]		8.5	ns
t_{GTSA}(1)	Global 3-state enable		40.0	ns
t_{GTSR}(1)	Global 3-state disable		40.0	ns
t_{RR}(1)	Input to register reset		11.0	ns
t_{RP}(1)	Input to register preset		11.0	ns
t_{GRR}(1)	Global reset to register reset		40	ns
t_{GZIA}(1)	Global ZIA delay		4.5	ns

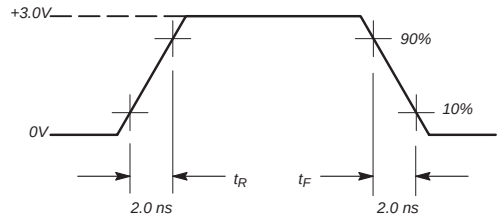
Note 1: This parameter is guaranteed by design and characterization, not by test.
Note 2: Output C_L = 5.0 pF.

Thevenin Equivalent



SP00629

Voltage Waveform



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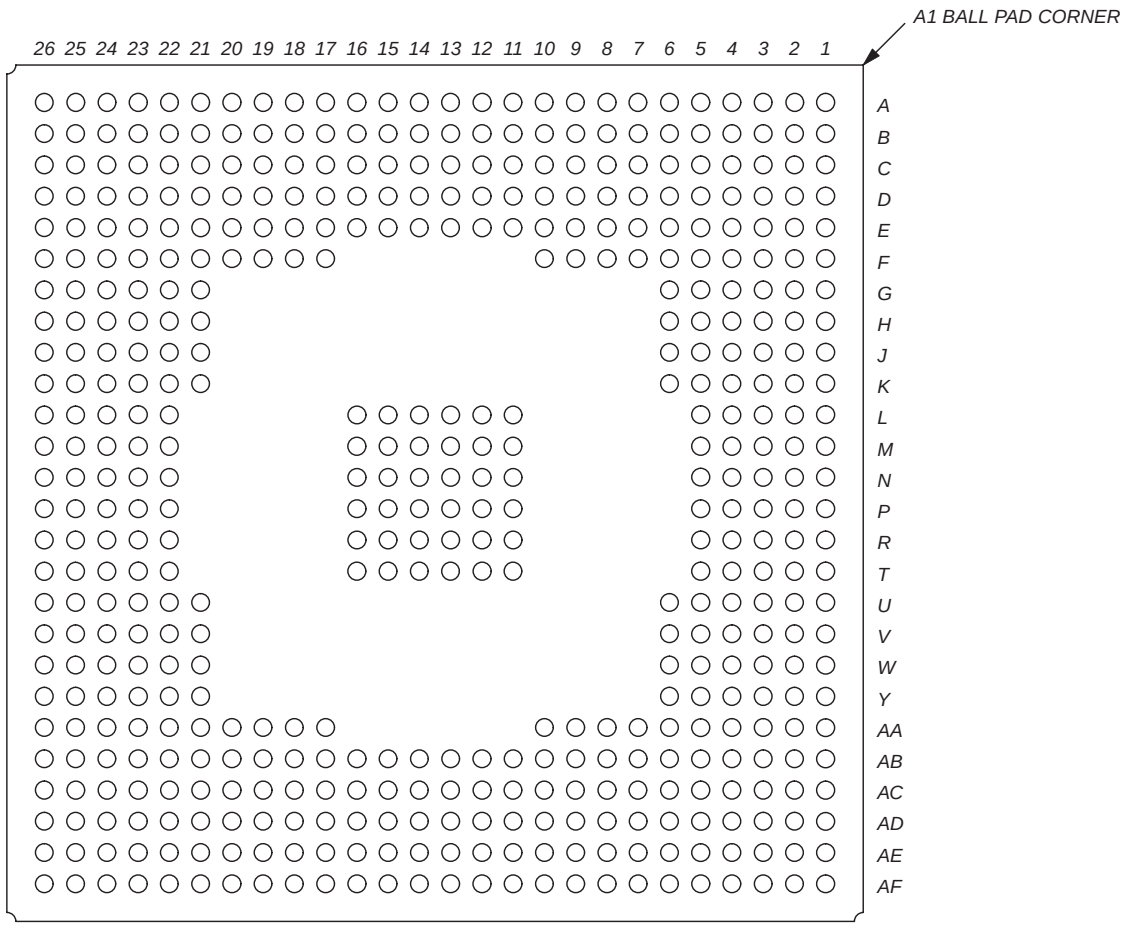
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Package Diagram for XCR3960

XCR3960 - 492-pin Plastic BGA



BOTTOM VIEW

SP00614

Pinouts for XCR3960

Function is Fast Module_Logic block_Macrocell. For example, F1_0_5 means Fast Module 1, Logic block 0, Macrocell.5

Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball
F1_0_5	A1	F1_0_1	B1	F1_1_14	C1	F1_1_12	D1
F1_0_7	A2	F1_0_2	B2	F1_0_0	C2	F1_1_13	D2
F1_2_22	A3	F1_2_23	B3	F1_0_4	C3	F1_1_15	D3
F1_2_19	A4	F1_2_20	B4	F1_2_21	C4	F1_0_3	D4
F1_3_30	A5	F1_3_31	B5*	F1_2_16	C5	F1_2_18	D5
F1_3_26	A6	F1_3_27	B6	F1_3_28	C6	F1_3_29	D6
F2_1_10	A7	F2_1_9	B7	F2_1_8	C7*	F1_3_24	D7
F2_1_15	A8	F2_1_13	B8	F2_1_12	C8	F2_1_11	D8
F2_0_3	A9	F2_0_2	B9	F2_0_1	C9	F2_0_0	D9
F2_2_23	A10	F2_0_7	B10	F2_0_5	C10	F2_0_4	D10
F2_2_19	A11	F2_2_22	B11	F2_2_21	C11	F2_2_20	D11
F2_2_17	A12	F2_2_18	B12	F2_3_31	C12*	F2_3_30	D12
F2_3_28	A13	F2_3_29	B13	F2_3_27	C13	F2_3_26	D13
F3_1_9	A14	F3_1_10	B14	F2_3_24	C14	F2_3_25	D14
F3_1_13	A15	F3_1_14	B15	F3_1_12	C15	F3_1_11	D15
F3_1_15	A16	F3_0_3	B16	F3_0_2	C16	F3_0_1	D16
F3_0_4	A17	F3_0_5	B17	F3_0_6	C17	F3_0_7	D17
F3_2_23	A18	F3_2_21	B18	F3_2_20	C18	F3_2_19	D18
F3_2_18	A19	F3_2_17	B19	F3_2_16	C19	F3_3_31	D19*
F3_3_29	A20	F3_3_28	B20	F3_3_27	C20	F3_3_26	D20
F3_3_25	A21	F3_3_24	B21	F4_1_8	C21*	F4_1_9	D21
F4_1_11	A22	F4_1_12	B22	F4_1_13	C22	F4_1_14	D22
F4_1_15	A23	F4_0_0	B23	F4_0_1	C23	F4_0_7	D23
F4_0_3	A24	F4_0_4	B24	F4_2_20	C24	F4_2_17	D24
F4_0_5	A25	F4_0_6	B25	F4_2_19	C25	F4_2_16	D25
F4_2_23	A26	F4_2_21	B26	F4_2_18	C26	F4_3_31	D26*

* Multi-function pin used during configuration. See Table 15 for information.

Function is Fast Module_Logic block_Macrocell. For example, F1_0_5 means Fast Module 1, Logic block 0, Macrocell.5

Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball
F1_1_8	E1*	F0_3_28	F1	F0_2_17	G1	F0_2_22	H1
F1_1_9	E2	F0_3_27	F2	F0_2_16	G2	F0_2_21	H2
F1_1_10	E3	F0_3_25	F3	F0_3_30	G3	F0_2_19	H3
F1_1_11	E4	F0_3_24	F4	F0_3_29	G4	F0_2_18	H4
GND	E5	V_{CC}	F5	V_{CC}	G5	F0_0_5	H5
F1_0_6	E6	F6 GND	F6	V_{CC}	G6	F0_1_15	H6
F1_3_25	E7	F1_2_17	F7	V_{CC}	G21	F5_3_31	H21
F2_0_6	E8	F2_1_14	F8	V_{CC}	G22	F5_2_21	H22
V_{CC}	E9	V_{CC}	F9	F5_1_9	G23	F5_1_14	H23
F2_2_16	E10	V_{CC}	F10	F5_1_11	G24	F5_0_0	H24
V_{CC}	E11	V_{CC}	F17	F5_1_12	G25	F5_0_1	H25
V_{CC}	E12	V_{CC}	F18	F5_1_13	G26	F5_0_2	H26
F3_1_8	E13*	F3_3_30	F19	-	-	-	-
V_{CC}	E14	F4_0_2	F20	-	-	-	-
V_{CC}	E15	GND	F21	-	-	-	-
F3_0_0	E16	V_{CC}	F22	-	-	-	-
V_{CC}	E17	F4_3_26	F23	-	-	-	-
V_{CC}	E18	F4_3_25	F24	-	-	-	-
F3_2_22	E19	F4_3_24	F25	-	-	-	-
F4_1_10	E20	F5_1_8	F26	-	-	-	-
F4_2_22	E21	-	-	-	-	-	-
GND	E22	-	-	-	-	-	-
F4_3_30	E23	-	-	-	-	-	-
F4_3_29	E24	-	-	-	-	-	-
F4_3_28	E25	-	-	-	-	-	-
F4_3_27	E26	-	-	-	-	-	-
F0_0_4	J1	F0_0_0	K1	F0_1_11	L1	F0_1_8	M1*
F0_0_6	J2	F0_0_1	K2	F0_1_14	L2	F0_1_10	M2
F0_0_7	J3	F0_0_2	K3	F0_1_13	L3*	CLK0	M3
F0_2_23	J4	F0_0_3	K4	F0_1_12	L4	CLK1	M4
F0_2_20	J5	V_{CC}	K5	F0_1_9	L5	V_{CC}	M5
F0_3_26	J6	F0_3_31	K6	GND	L11	GND	M11
F5_1_10	J21	F5_1_15	K21	GND	L12	GND	M12
F5_0_4	J22	V_{CC}	K22	GND	L13	GND	M13
F5_0_3	J23	F5_2_23	K23	GND	L14	GND	M14
F5_0_5	J24	F5_2_22	K24	GND	L15	GND	M15
F5_0_6	J25	F5_2_20	K25	GND	L16	GND	M16
F5_0_7	J26	F5_2_19	K26	V_{CC}	L22	F5_3_25	M22
-	-	-	-	F5_2_16	L23	F5_3_26	M23
-	-	-	-	F5_2_17	L24	F5_3_27	M24
-	-	-	-	F5_2_18	L25	F5_3_29	M25
-	-	-	-	F5_3_30	L26	F5_3_28	M26

* Multi-function pin used during configuration. See Table 15 for information.

Function is Fast Module_Logic block_Macrocell. For example, F1_0_5 means Fast Module 1, Logic block 0, Macrocell.5

Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball
CLK3	N1	TDI	P1	F11_3_28	R1	F11_3_30	T1
CLK2	N2	F11_3_24	P2	F11_3_29	R2	F11_2_18	T2
TRSTN	N3	TDO	P3	F11_3_27	R3*	F11_2_17	T3
TMS	N4	TCK	P4	F11_3_26	R4	F11_2_16	T4
GTS	N5	V_{CC}	P5	F11_3_25	R5	V_{CC}	T5
GND	N11	GND	P11	GND	R11	GND	T11
GND	N12	GND	P12	GND	R12	GND	T12
GND	N13	GND	P13	GND	R13	GND	T13
GND	N14	GND	P14	GND	R14	GND	T14
GND	N15	GND	P15	GND	R15	GND	T15
GND	N16	GND	P16	GND	R16	GND	T16
V_{CC}	N22	DONE	P22	V_{CC}	R22	F6_1_8	T22
RESETN	N23	PRGMN	P23	CLK5	R23	F6_1_12	T23
GND	N24	CCLK	P24	CLK4	R24	F6_1_13	T24
F5_3_24	N25	CLK6	P25	F6_1_10	R25	F6_1_14	T25
GND	N26	CLK7	P26	F6_1_9	R26	F6_1_11	T26
F11_2_19	U1	F11_0_7	V1	F11_0_2	W1	F11_1_13	Y1*
F11_2_20	U2	F11_0_6	V2	F11_0_1	W2	F11_1_12	Y2
F11_2_22	U3	F11_0_4	V3	F11_0_0	W3	F11_1_11	Y3
F11_2_23	U4	F11_0_3	V4	F11_1_14	W4	F11_1_9	Y4
V_{CC}	U5	F11_0_5	V5*	F11_2_21	W5	V_{CC}	Y5
F11_1_15	U6	F11_1_10	V6	F11_3_31	W6*	V_{CC}	Y6
F6_3_31	U21	F6_3_26	V21	F6_1_15	W21	V_{CC}	Y21
V_{CC}	U22	F6_2_21	V22	F6_0_5	W22	V_{CC}	Y22
F6_0_3	U23	F6_2_23	V23	F6_2_18	W23	F6_3_29	Y23
F6_0_2	U24	F6_0_7	V24	F6_2_19	W24*	F6_3_30	Y24
F6_0_1	U25	F6_0_6	V25	F6_2_20	W25	F6_2_16	Y25
F6_0_0	U26	F6_0_4	V26	F6_2_22	W26	F6_2_17	Y26

* Multi-function pin used during configuration. See Table 15 for information.

Function is Fast Module_Logic block_Macrocell. For example, F1_0_5 means Fast Module 1, Logic block 0, Macrocell.5

Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball
F11_1_8	AA1*	F10_3_27	AB1	F10_3_31	AC1*	F10_2_18	AD1
F10_3_24	AA2	F10_3_28	AB2	F10_2_16	AC2	F10_2_19	AD2
F10_3_25	AA3	F10_3_29	AB3	F10_2_17	AC3	F10_2_20	AD3
F10_3_26	AA4	F10_3_30	AB4	F10_0_7	AC4	F10_0_1	AD4
V_{CC}	AA5	GND	AB5	F10_1_14	AC5	F10_1_13	AD5*
GND	AA6	F10_2_22	AB6	F10_1_9	AC6	F10_1_8	AD6*
F10_0_2	AA7	F10_1_10	AB7	F9_3_26	AC7	F9_3_27	AD7*
F9_3_30	AA8	F9_2_22	AB8	F9_3_31	AC8*	F9_2_16	AD8
V_{CC}	AA9	V_{CC}	AB9	F9_2_19	AC9*	F9_2_20	AD9
V_{CC}	AA10	V_{CC}	AB10	F9_0_7	AC10	F9_0_6	AD10
V_{CC}	AA17	F9_0_0	AB11	F9_0_1	AC11	F9_0_2	AD11
V_{CC}	AA18	V_{CC}	AB12	F9_1_11	AC12	F9_1_12	AD12
F8_1_14	AA19	V_{CC}	AB13	F8_3_25	AC13	F9_1_8	AD13*
F7_2_17	AA20	F8_3_24	AB14	F8_3_26	AC14	F8_3_27	AD14*
GND	AA21	V_{CC}	AB15	F8_3_30	AC15	F8_3_31	AD15*
V_{CC}	AA22	V_{CC}	AB16	F8_2_20	AC16	F8_2_21	AD16
F6_3_24	AA23	F8_2_17	AB17	F8_0_4	AC17	F8_0_5	AD17*
F6_3_25	AA24	V_{CC}	AB18	F8_0_0	AC18	F8_0_1	AD18
F6_3_27	AA25	F8_0_6	AB19	F8_1_11	AC19	F8_1_12	AD19
F6_3_28	AA26	F7_3_26	AB20	F7_3_24	AC20	F8_1_8	AD20*
-	-	F7_0_6	AB21	F7_3_29	AC21	F7_3_28	AD21
-	-	GND	AB22	F7_2_18	AC22	F7_2_16	AD22
-	-	F7_1_11	AB23	F7_0_3	AC23	F7_2_21	AD23
-	-	F7_1_10	AB24	F7_1_14	AC24	F7_0_7	AD24
-	-	F7_1_9	AB25	F7_1_13	AC25	F7_0_0	AD25
-	-	F7_1_8	AB26	F7_1_12	AC26	F7_1_15	AD26

* Multi-function pin used during configuration. See Table 15 for information.

Function is Fast Module_Logic block_Macrocell. For example, F1_0_5 means Fast Module 1, Logic block 0, Macrocell.5

Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball
F10_2_21	AE1	F10_2_23	AF1	-	-	-	-
F10_0_6	AE2	F10_0_5	AF2*	-	-	-	-
F10_0_4	AE3	F10_0_3	AF3*	-	-	-	-
F10_0_0	AE4	F10_1_15	AF4	-	-	-	-
F10_1_12	AE5	F10_1_11	AF5	-	-	-	-
F9_3_24	AE6	F9_3_25	AF6	-	-	-	-
F9_3_28	AE7	F9_3_29	AF7	-	-	-	-
F9_2_17	AE8	F9_2_18	AF8	-	-	-	-
F9_2_21	AE9	F9_2_23	AF9*	-	-	-	-
F9_0_5	AE10*	F9_0_4	AF10	-	-	-	-
F9_0_3	AE11*	F9_1_15	AF11	-	-	-	-
F9_1_14	AE12	F9_1_13	AF12*	-	-	-	-
F9_1_10	AE13	F9_1_9	AF13	-	-	-	-
F8_3_29	AE14	F8_3_28	AF14	-	-	-	-
F8_2_18	AE15	F8_2_16	AF15	-	-	-	-
F8_2_22	AE16	F8_2_19	AF16*	-	-	-	-
F8_0_7	AE17	F8_2_23	AF17*	-	-	-	-
F8_0_2	AE18	F8_0_3	AF18*	-	-	-	-
F8_1_13	AE19*	F8_1_15	AF19	-	-	-	-
F8_1_9	AE20	F8_1_10	AF20	-	-	-	-
F7_3_27	AE21*	F7_3_25	AF21	-	-	-	-
F7_3_31	AE22*	F7_3_30	AF22	-	-	-	-
F7_2_20	AE23	F7_2_19	AF23*	-	-	-	-
F7_2_23	AE24*	F7_2_22	AF24	-	-	-	-
F7_0_2	AE25	F7_0_5	AF25	-	-	-	-
F7_0_1	AE26	F7_0_4	AF26	-	-	-	-

* Multi-function pin used during configuration. See Table 15 for information.

Pin Description

Table 15: Pin Description

Symbol	Pin Number	Type	Description
V_{CC}	E9, E11, E12, E14, E15, E17, E18, F5, F9, F10, F17, F18, F22, G5, G6, G21, G22, K5, K22, L22, M5, N22, P5, R22, T5, U5, U22, Y5, Y6, Y21, Y22, AA5, AA9, AA10, AA17, AA18, AA22, AB9, AB10, AB12, AB13, AB15, AB16, AB18	-	Positive power supply.
GND	E5, E22, F6, F21, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N11, N12, N13, N14, N15, N16, N24, N26, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, AA6, AA21, AB5, AB22	-	Ground supply.
RESETN	N23	I	During configuration, RESETN forces the start of initialization (see Figure 9). After configuration, RESETN is a direct input which can be used to asynchronously reset all the flip-flops. If the global reset is not being used, this pin should be pulled High. If the rise time of the PRGMN signal is greater than 1 µs, this signal must be held Low until PRGMN is High.
CCLK	P24	I/O	In the master modes, CCLK is an output which strobes configuration data in. In the slave or synchronous peripheral mode, CCLK is an input synchronous with the data on DIN or D[7:0]. After configuration, this pin should be pulled Low.
DONE	P22	I/O	DONE is a bidirectional signal with a weak pull-up resistor attached. As an output, DONE pulling High indicates configuration is complete. As an input, a low level on DONE will delay the enabling of user I/O. If only one device is used, this pin can be left floating. If multiple devices are daisy-chained, an external pull-up should be used (see Figure 27).
PRGMN	P23	I	PRGMN is an active Low input that forces the restart of configuration and initialization (see Figure 9) and resets the boundary-scan circuitry. After configuration, the pin should be pulled High. This signal must have a rise time less than 1 µs. If the rise time of this signal is greater than 1 µs, RESETN must be held Low until PRGMN is High.
SPMI	E13	O	Special purpose configuration pin that must be left floating during configuration for all configuration modes. After configuration the pin is a user-programmable I/O, and no external termination is required. See “Terminations” on page 8.
MPMI	C12	O	Special purpose configuration pin that must be left floating during configuration for all configuration modes. After configuration the pin is a user-programmable I/O, and no external termination is required. See “Terminations” on page 8.

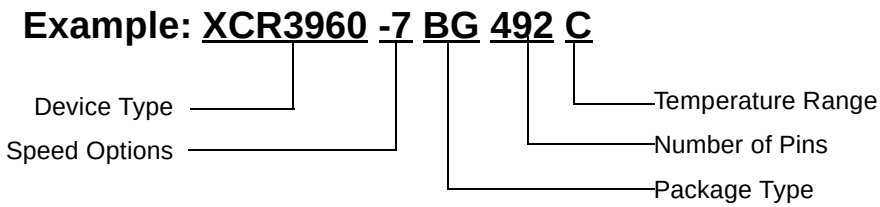
Table 15: Pin Description (Continued)

Symbol	Pin Number	Type	Description
DIN	AC1	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D[0] input. After configuration, the pin is a user-programmable I/O, and no external termination is required. See “Terminations” on page 8.
M2	AE22	I	M2/M1/M0 are used to select the configuration mode as defined in Table 3. After configuration, the pins are user-programmable I/O, and no external termination is required. See “Terminations” on page 8.
M0	AE24		
M1	AF23		
M3	AD20	I	M3 should be pulled High during configuration for all configuration modes. After configuration, the pin is a user-programmable I/O, and no external termination is required. See “Terminations” on page 8.
TDI TDO TCK TMS TRSTN	P1 P3 P4 N4 N3	I O I I I	Test Data In, Test Data Out, Test Clock, Test Mode Select, Test Reset are dedicated pins for boundary-scan through the JTAG port. If JTAG is not being used, TDI, TCK, TMS, and TRSTN should be terminated with a weak pull-up resistor. TDO can be left unterminated. See “Terminations” on page 8.
HDC	C21	O	High During Configuration (HDC) is output High when the XCR3960 is in the configuration state. HDC is used as a control output indicating that configuration is in progress. After configuration, the pin is a user-programmable I/O, and no external termination is required. See “Terminations” on page 8.
LDCN	D19	O	Low During Configuration (LDCN) is output Low when the XCR3960 is in the configuration state. LDCN is used as a control output indicating that configuration is in progress. After configuration, the pin is a user-programmable I/O, and no external termination is required. See “Terminations” on page 8.
CRCerrn	D26	I/O	CRCerrn goes Low when the XCR3960 detects a CRC error or an invalid peramble during configuration. The XCR3960 that detected the error will go into the initialization state and will not resume configuration until PRGMN and RESETN are both High. Once configuration has resumed CRCerrn will go High. During configuration, an internal pull-up is enabled. If only one device is used, this pin can be left floating. If multiple devices are daisy-chained, an external pull-up should be used (see Figure 27). After configuration, the pin is a user-programmable I/O, and no external termination is required. See “Terminations” on page 8.
GTS	N5	I	Global 3-state is an active High dedicated input used to 3-state the I/Os and activate the internal pull-down resistors. If this feature is not used, the pin should be pulled Low.
CS0N CS1 WRN	B5 C7 E1	I	CS0N/CS1/WRN are used in the peripheral configuration mode. The XCR3960 is selected when CS0N and WRN are low and CS1 is High. After configuration, these pins are user-programmable I/O. CS0N and WRN require no external termination. See the section on terminations for more information. If CS1 is not used as an I/O after configuration in synchronous peripheral mode, the 3-state property should be used to disable the internal pull-down resistor. See “Synchronous Peripheral Mode” on page 20.

Table 15: Pin Description (Continued)

Symbol	Pin Number	Type	Description
A[19:0]	AF2, AF3, AD5, AD6, AD7, AC8, AC9, AF9, AE10, AE11, AF12, AD13, AD14, AD15, AF16, AF17, AD17, AF18, AE19, AE21	O	In the master parallel configuration mode, A[19:0] address the configuration EEPROM. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8.
D[7:0]	L3, M1, R3, W6, V5, Y1, AA1, AC1	I	During master parallel, peripheral, and slave parallel configuration modes, D[7:0] receive configuration data. After configuration, the pin is a user-programmable I/O and no external termination is required. See "Terminations" on page 8.
dout	W24	O	During configuration, dout is the serial data out that is used to drive the DIN of daisy-chained slave devices. Data on DOUTchanges on the falling edge of CCLK. After configuration, the pin is a user-programmable I/O and no external termination is required. See "Terminations" on page 8.

Ordering Information



Speed Options
-8: 8 ns pin-to-pin delay
-7: 7.5 ns pin-to-pin delay

Temperature Range
C = Commercial, T_A = 0°C to +70°C
I = Industrial, T_A = –40°C to +85°C

Packaging Options
BG492: 492-ball BGA

Component Availability

Pins		492
Type		Plastic BGA
Code		BG492
XCR3960	-8	I
	-7	C

Revision History

Date	Version	Revision
9/15/99	1.0	Xilinx release of document.
2/10/00	1.1	Converted to Xilinx format and updated.
8/28/00	1.2	Added note to Electrical Characteristics tables
10/09/00	1.3	Added Product Discontinuation Notice.