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CoolRunner XPLA3 Clocking Options

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Summary

This document gives a detailed description of the CoolRunner® XPLA3 clocking options.

Introduction

For today's complex systems, designers often require multiple clocking options from their CPLDs. This document describes how the CoolRunner XPLA3 CPLDs address this need. The CoolRunner XPLA3 family includes versatile clocking options that include both synchronous (external) and asynchronous (internal, equation based) clocking and selectable polarity at every macrocell.

A brief overview of the XPLA3 architecture as it pertains to the clocking features will be described in the following sections. The XPLA3 architecture will not be fully described in this white paper. For more details on the XPLA3 architecture, please refer to white paper WP105, "CoolRunner XPLA3 CPLD Architecture Overview".

CoolRunner XPLA3 Architecture

The CoolRunner XPLA3 architecture consists of logic blocks that are interconnected by a routing matrix called the Zero-power Interconnect Array (ZIA). Each logic block contains 16 macrocells. The block diagram for a 64 macrocell device is shown in Figure 1. There are four universal control terms available to all logic blocks in a XPLA3 CPLD: a Universal Clock (UCLK), a Universal Reset (URST), a Universal Preset (UPST), and a Universal Output Enable (UOE). One control term from each logic block is routed to a set of multiplexers that generates the four Universal Control Terms. The Universal Control Terms are then routed to each logic block for use by the macrocells.

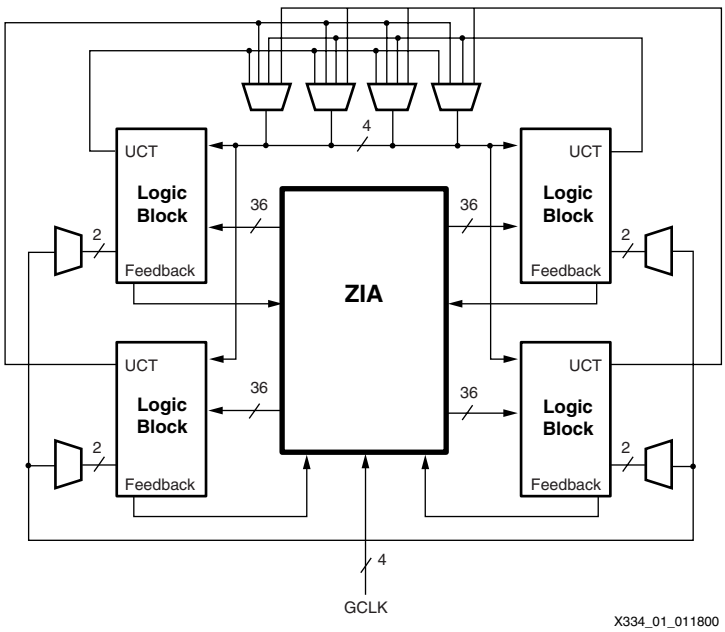

Figure 1: **XPLA3 High-Level Architecture (64 macrocell device shown)**

Each logic block contains a pure PLA array (programmable AND, programmable OR). The PLA array provides a pool of 48 product terms that can be used as macrocell clocks, control terms (reset, preset, clock-enables, or output-enables), or as needed by the 16 macrocells in the logic block. The first eight product terms in the PLA are used to generate eight Local Control Terms (LCT[0:7]). Note that if these product terms are not needed as control terms, they are available for other logic. Local Control Term 7 (LCT7) is routed from the logic block to the universal control term multiplexers.

As seen in Figure 2, both Local and Universal Control Terms can be used in the macrocell as the macrocell register clock, reset, and preset functions as well as the output enable for the output buffer. In addition, Local Control Terms can be used as hardware clock enables.

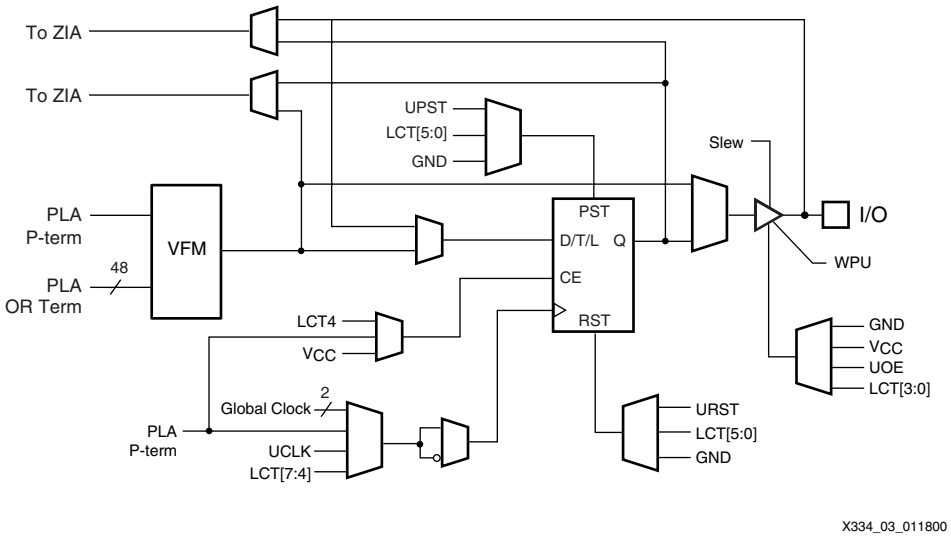

Figure 2: **XPLA3 Macrocell**

XPLA3 Clocking Options

All CoolRunner XPLA3 CPLDs provide multiple clock sources to each register of the device. These sources include both synchronous and asynchronous clocking. Each type of clock source has well defined capabilities, depending upon whether the clock is generated from an input or from an equation. Each XPLA3 macrocell register can be clocked from any one of the following ten sources:

- There are two global synchronous clocks per logic block that are derived from the four external clock pins via a 4:2 multiplexer.
- There is one Universal Clock Signal (UCT0) sourced by a Universal Control Term.
- There are four Local Control Terms (LCT[4:7]) which can be used as clock signals. These clocks can be individually configured as either a product term or sum term equation created from the 36 signals available inside the logic block.
- There is one dedicated Product Term Clock per macrocell.

The sections below describe these various types of clocking sources. Please note that all of these clock sources provide low skew signals.

Global Synchronous Clocks

The first type of clock source is associated with dedicated input pins. As shown in Figure 1, these inputs are attached directly to a low skew, dedicated clock network. These clock networks can be driven in a synchronous (external) fashion only. The polarity of these clocks is selectable at every macrocell. All of the XPLA3 devices have four global clock sources with two of the four being selectable for use in each logic block. It is worth noting that the input may be used as both an input to the logic array (via the ZIA interconnect) and as a global clock at the

same time. Thus, this input can be used as both a clock and as a signal in the design simultaneously. The Global Synchronous Clocks provide the highest possible design frequency clocks within the CPLD.

Universal Control Term Clock

There is one Universal Clock Signal (UCT0) sourced by a Universal Control Term. This universal clock signal is accessible by every macrocell flip-flop in the device. Many designs require that a product term based clock be used for large portions of the CPLD design. These designs greatly benefit from the use of the Universal Clock Control Term (UCLK).

One example of this type of application is where the CPLD implements an I^2C controller along with a microcontroller interface as shown in Figure 3. The clock provided by the micro-controller or by the system is typically much faster than that needed to drive the I^2C bus. A large portion of the CPLD design will be clocked from the system clock and the portion of the CPLD logic interfacing to the I^2C bus will be clocked by a divided version of the system clock.

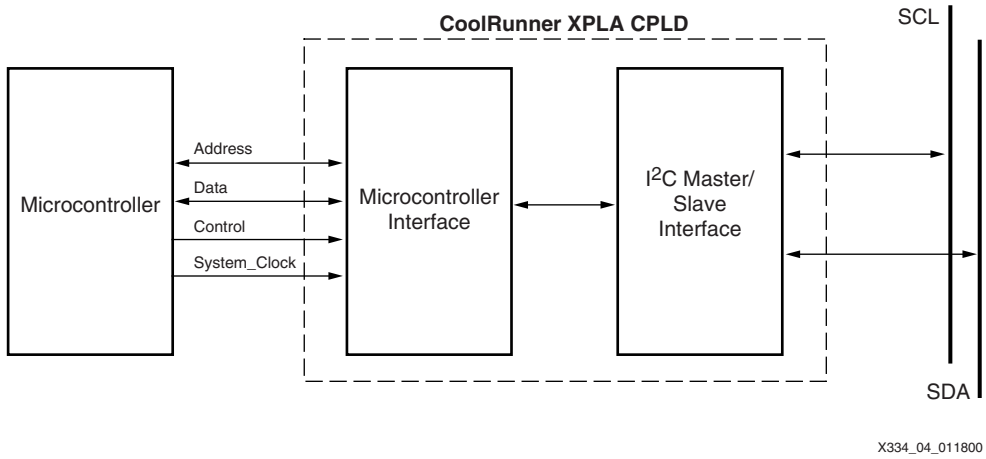

Figure 3: **CoolRunner I^2C Bus Controller**

In this case, a counter is used to divide the system clock to the 100 KHz (or 400 KHz) clock needed to drive the I^2C clock (SCL). Since an I^2C controller can both send and receive data, the I^2C portion of the CPLD logic will also need to be clocked by SCL. Therefore, the output of the counter that produces SCL will not only be output from the CPLD, but will also be routed on the universal clock signal (UCLK) to clock internal portions of the CPLD logic that interface to the I^2C bus. Routing SCL on UCLK saves Local Control Terms, product terms, and fan-in to logic blocks.

There is an additional delay associated with the Universal Control Term, therefore, the Universal Control Term Clock provides the slowest possible system frequency clocks within the CPLD. For additional timing information, refer to WP122, "Using the CoolRunner XPLA3 Timing Model".

Local Control Term Clocks

The third type of clock source is provided by the control terms in each logic block. There are four Local Control Terms (LCT[4:7]) which can be used as a clock signal and can be individually configured as either a product term or sum term equation created from the 36 signals available inside the logic block. Local Control Term 4 and 5 (LCT4 and LCT5) are also shared by Macrocell Reset and Preset with LCT4 also being shared by Clock Enable. If asum-of-products equation is required, it must be implemented in a macrocell and then fed-back into a control term through the ZIA.

Each Local Control Term Clock is available to all the macrocells within a logic block, but it must be duplicated on another control term if the same clock is used in different logic blocks. In this

case, it might be better to use the Universal Control Term Clock. Local Control Term clocks are not attached to a low-skew clock network but are excellent for implementing a commonly used product term based clock. The Local Control Term Clocks and the Product Term Clocks (described in the section below) support system frequencies faster than the Universal Control Term Clocks and slower than the Global Control Term Clocks.

Product Term Clocks

The fourth type of clock source provided is a dedicated Product Term Clock for each macrocell. These clocks can be individually configured as a product term equation created from the 36 signals available inside the logic block. These clocks are not attached to a low-skew clock network and must be duplicated if this Product Term Clock is used to clock multiple flip-flops. In this case, it might be better to use either a Local or Universal Control Term Clock. Product Term Clocks have the advantage of being available at every macrocell. This elimates all routing restraints on the clock and allows the user the flexibility to implement the logic anywhere on the device.

Additional Clocking Features

In addition to having ten possible clock sources, polarity (rising or falling edge) is also selectable per macrocell. Hardware Clock Enables are also available for added clock control. Clock Enables can be controlled by a Local Control Term (LCT4) or by a dedicated Product Term.

Conclusion

This white paper describes the CoolRunner XPLA3 clocking options. Timing associated with these various clocking options is described in WP122, "Using the CoolRunner XPLA3 Timing Model".

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/13/00	1.0	Initial Xilinx release.