C8251 Programmable Communication Interface

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Features

- Based on the Intel 8251A device
- Pre-defined implementation for predictable timing
- Verified against a hardware model of the original device
- Synchronous and asynchronous operation
- Programmable data word length, parity and stop bits
- Parity, overrun and framing error checking instructions and counting loop interactions
- Divide-by 1,-16,-64 mode
- False start bit deletion
- Automatic break detection
- Internal and external synch character detection
- Peripheral modem control functions

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core design document
Design File Formats	XNF Netlist VHDL Source RTL
Constraints File	C8251.ucf
Verification	VHDL Testbench, test vectors
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	None
Additional Items	None
Simulation Tool Used	
1076-compliant VHDL simulator, Verilog simulator	
Support	
Support provided by CAST, Inc.	

Applications

The C8251 core is used in communication and modem applications.

Table 1: Core Implementation Data

Supported Family	Device Tested	CLB Slices[2]	Clock IOBs[1]	IOBs[1]	Performance (MHz)	Xilinx Tools	Special Features
Virtex	V50-6	268	4	31	46	M2.1i	None
Virtex-E	V50E-8	268	4	31	54	M2.1i	None
Spartan-II	2S50-6	268	4	31	43	M2.1i	None

Notes:
1. Assuming all core I/Os are routed off-chip.
2. Optimized for speed.

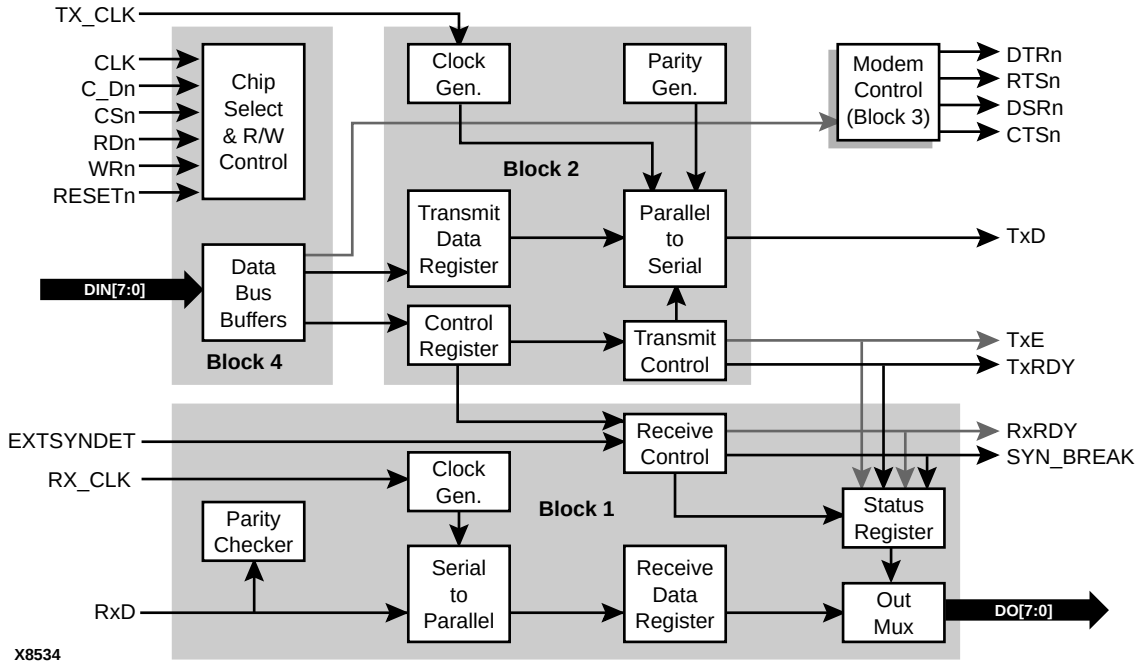

Figure 1: C8251 Programmable Communication Interface Block Diagram

General Description

The C8251 programmable communications interface (USART) core provides data formatting and control to a serial communication channel.

The core has select, read/write, interrupt and bus interface logic features that allow data transfers over an 8-bit bi-directional parallel data bus system. With proper formatting and error checking, the core can transmit and receive serial data, supporting both synchronous and asynchronous operation.

Functional Description

The C8251 core is partitioned into modules as shown in Figure 1 and described below.

Block 1

The Receiver Buffer and Control accepts serial data, converts it to parallel format, checks for parity, framing, overrun, and break, and sends the formatted data to the CPU.

Block 2

The Transmitter Buffer and Control logic accepts parallel data from the Data Bus Buffer, converts it to serial, inserts required characters or bits depending on the communication protocol, and outputs the formatted serial stream to the TxD output pin.

Modem Control Logic (Block 3)

This consists of a set of inputs and outputs that can be used to interface to almost any modem.

Block 4

The CPU interface shares common interface signals with the CPU: Data Bus, Read, Write, Chip selects, Reset and Master CLK.

Core Modifications

The C8251 core can be customized to include:

- 16 bit Internal Baud Rate Generator
- Remove either synchronous or asynchronous sections in order to reduce area

Please contact CAST directly for any required modifications.

Pinout

The pinout of the C8251 core has not been fixed to specific FPGA I/O, allowing flexibility with a users application. Signal names are shown in the block diagram in Figure 1 and described in Table 2.

Core Assumptions

- Active-low reset input
- Does not support 1.5 stop bit mode
- EXTSYNDET and SYN_BREAK signals are separate
- The bi-directional data bus has been split in two separate data buses: DIN and DO

Verification Methods

The C8251 USART core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model which contained the original Intel 8251A chip, and the results compared with the core's simulation outputs.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

The C8251 core is available from CAST, Inc. Please contact CAST, Inc. directly for pricing and information. The core is licensed from Moxsyn S.r.l.

Related Information

Intel Microcommunications Data Book

Intel order number: 231658
ISBN: 1-55512-148-9
Document number: 205222-002
Contact:
Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641
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Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Table 2: Core Signal Pinout

Signal	Signal Direction	Description
I/O Signals		
C_Dn	Input	Control/Data Select
CSn	Input	Chip Select
RDn	Input	Read control
RESETn	Input	External reset
DIN[7:0]	Input	Data Input Bus
EXTSYNDET	Input	External synch detect
RxD	Input	Receive Data
DTRn	Output	Data Terminal Ready
RTSn	Output	Request-to-Send
DSRn	Input	Data Set Ready
CTSn	Input	Clear-to-Send
TxD	Output	Transmit Data
TxE	Output	Transmitter empty
TxRDY	Output	Transmit ready
RxRDY	Output	Receiver ready
SYN_BREAK	Output	Sync/Break detect
D0[7:0]	Output	Data Output Bus
Signals using CLKIOB Pins		
TX_CLK	Input	Transmit clock
CLK	Input	Master clock
WRn	Input	Write control
RX_CLK	Input	Receive clock