C8051 Microcontroller

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Features

- Supports Virtex™, Virtex™-E and Spartan®-II devices
- 8-Bit Control Unit
- 8-Bit Arithmetic-Logic Unit
- 32-bit Input/Output
- Two 16-bit Timer/Counters
- Serial Peripheral Interfaces in full duplex mode
- Two priority Interrupt Controllers
- Internal Data Memory interface can address up to 256 K bytes of Read/Write data memory space
- External Memory interface can address up to 64 K bytes of external program memory space and up to 64 K bytes of external data memory space
- Special Function Registers interface

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core Specification, Instruction set details, Tests set details
Design File Formats	.ngo, EDIF Netlist, VHDL or Verilog Source RTL available at extra cost
Constraints File	C8051.ucf
Verification	VHDL testbench
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	Example design, assembler programs
Additional Items	Simulation and synthesis scripts
Simulation Tool Used	
1076-compliant VHDL Simulator, Verilog Simulator	
Support	
Support provided by CAST, Inc.	

Applications

- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and video

Table 1: Core Implementation Data

Supported Family	Device Tested	CLB Slices[1]	Clock IOBs[2]	IOBs[2]	Performance (MHz)	Xilinx Tools	Special Features
Spartan-II	2S150-6	1218	1	142	57	M3.2i	None
Virtex	V100-6	1218	1	142	57	M3.2i	None
Virtex-E	V200E-8	1218	1	142	68	M3.2i	None

Notes:
1. Optimized for speed
2. Assuming all core I/Os are routed off-chip

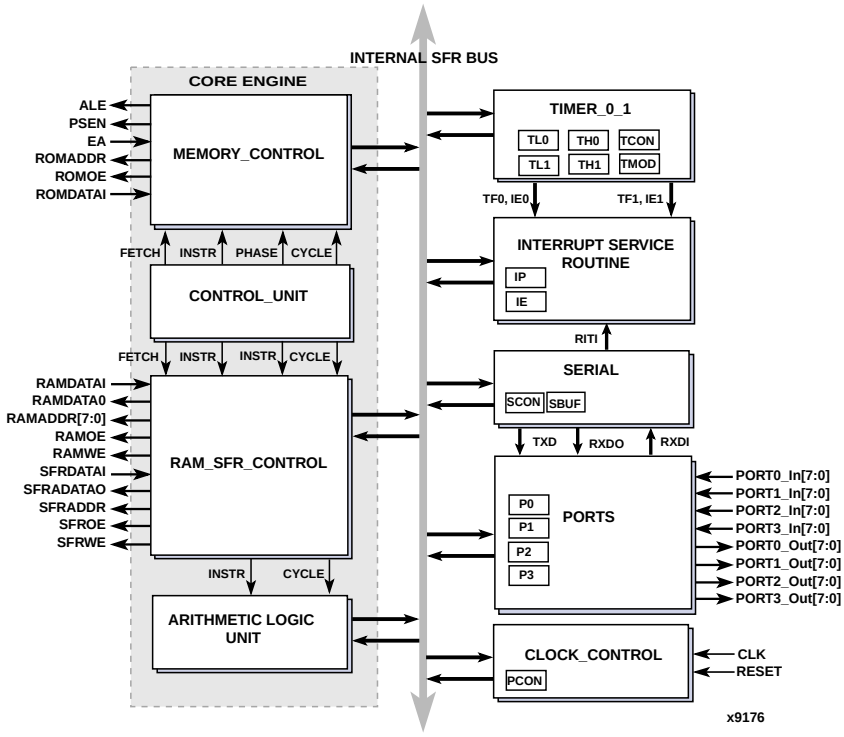

Figure 1: C8051 Microcontroller Block Diagram

General Description

The C8051 is a core of a fast single-chip 8-bit microcontroller. The C8051 is a fully functional 8-bit embedded controller that executes all ASM51 instructions and has the same instruction set as the Intel 80C31. The C8051 serves software and hardware interrupts, provides an interface for serial communications, and a timer system.

The C8051 is a microcode-free design developed for reuse in FPGA implementations. The design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset.

Functional Description

The C8051 core is partitioned into modules as shown in Figure 1 and described below.

Core Engine

The C8051 engine is composed of four components:

- Memory control unit
- Control unit
- RAM and SFR control unit
- Arithmetic-logic unit

The C8051 engine allows to fetch instruction from program memory and to execute using RAM or SFR.

Memory Control Unit

- Can address up to 64 K bytes of External Program Memory Space
- Can address up to 64 K bytes of External Data Memory Space

Control Unit

The Control Unit performs instruction fetch and execution from the Memory Control Unit and the RAM_SFR Control Unit.

RAM and SFR Control Unit

- Can address up to 256 bytes of Read/Write Data Memory Space
- Serves the Interface for off-core Special Function Registers

Arithmetic-logic Unit

- 8 bit arithmetic operations
- 8 bit logical operations
- Boolean manipulations

- 8 x 8 bit multiplication
- 8 / 8 bit division

Timer 0 and 1

Timers 0 and 1 are nearly identical. Timers 0 and 1 both have four modes. They are:

- 13-bit Timer/counter
- 16-bit Timer/counter
- 8-bit timer/counter with auto reload
- two 8-bit timers

The later mode is available to Timer 0 only. Each timer can also serve as a counter of external pulses (1 to 0 transition) on the corresponding T0 or T1 pin. One other option is to gate the timer/counter using an external control signal. This allows the timer to measure the pulse width of external signals.

Interrupt Service Routine

The C8051 core improves two-priority interrupt system. There are 5 interrupt sources. Each source has an independent priority bit, flag, interrupt vector, and enable. In addition, interrupts can be globally enabled or disabled.

Serial

The C8051 core provides interface for serial communication. The serial port is capable of both synchronous and asynchronous modes. In synchronous mode, the microcontroller generates the clock and operates in a half-duplex mode. In asynchronous mode, full duplex operation is available. Receive data is buffered in a holding register. This allows the serial to receive an incoming word before software has read the previous value.

The port provides four operating modes. These offer different communication protocols and baud rates:

- Synchronous mode, fixed baud rate
- 8-bit UART mode, variable baud rate
- 9-bit UART mode, fixed baud rate
- 9-bit UART mode, variable baud rate

Ports

The C8051 provides four I/O ports. Port 0 – Port 3 are an 8-bit bi-directional I/O ports with separated inputs and outputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memories.

Port 1 also serves the special features like external interrupt inputs, Serial 1 interface, and Timer 2 inputs.

Port 2 emits the high-order address byte during fetches from external program memory that use 16-bit addresses (MOVX @DPTR).

Port 3 also serves the special features like read and write strobes for external data memory, Serial 0 interface, Timer 0 and Timer 1 inputs.

Clock Control

The Clock Control unit generates the internal synchronous reset. It also contains registers for selecting the clock for timers.

Pinout

The pinout of the C8051 core has not been fixed to specific FPGA I/O, allowing flexibility with a users application. Signal names are shown in the block diagram in Figure 1, and in Table 2.

Table 2: Core Signal Pinout

Signal	Direction	Description
Internal Program Memory Interface		
ALE	Output	Address Latch Enable
PSEN	Output	Program Store Enable
EA	Input	External Access Enable
ROMADDR	Output	Memory Interface
ROMOE	Output	Data File Output Enable
ROMDATAI[7:0]	Output	Memory Data Bus Input
Internal Data Memory Interface		
RAMDATAI	Input	Memory data bus input
RAMDATAO	Output	Memory data bus output
RAMADDR	Output	Memory address bus
RAMWE	Output	Memory write enable
RAMOE	Output	Memory output enable
External Special Function Registers Interface		
SFRDATAI	Input	SFR data bus input
SFRDATAO	Output	SFR data bus output
SFRADDR	Output	SFR address bus
SFRWE	Output	SFR write enable
SFROE	Output	SFR output enable
Interrupt Service Routine		
PFI	Input	Power Failure Interrupt
Ports		
Port0I[7:0] Port0O[7:0]	Input Output	Port 0 Input Bus Port 0 Output Bus
Port1I[7:0] Port1O[7:0]	Input Output	Port 1 Input Bus Port 1 Output Bus
Port2I[7:0] Port2O[7:0]	InputI Output	Port 2 Input Bus Port 2 Output Bus
Port3I[7:0] Port3O[7:0]	Input Output	Port 3 Input Bus Port 3 Output Bus
Clock Control		
CLK	Input	Clock Input
RESET	Input	Hardware reset input

Core Modifications

The C8051 core can be modified to include features such as:

- Three 16-bit Timer/Counters
- Two Serial Peripheral Interfaces in full duplex mode
- 15-bit Programmable Watchdog Timer
- 32-bit Fast Multiplication-Division Unit
- 4x16-bit Compare/Capture Unit
- Real Time Clock
- EMI reduction mode disables ALE

Please contact CAST, Inc. directly for any required modifications.

C8051 Development Environment

- VHDL or Verilog source code for the C8051
- Synthesis support (Synopsys)
- A complete set of synthesis scripts
- Simulation support (Synopsys, MTI, Aldec)
- A set of scripts and macros
- Example CHIP_C8051 – 8051 compatible design
- This design uses the C8051 and illustrates how to build and connect memories and port modules
- Extensive HDL testbench that instantiates:
  - example design CHIP_C8051
  - external RAM
  - external ROM
  - clock generator
  - process that compares your simulation results with the expected results
- A collection of 8051 assembler programs which are executed directly by the testbench
- A set of expected results
- Additional documentation
  - Architectural overview
  - Hardware description
  - User Guide
- Design support including consulting

Verification Methods

The C8051 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C31 chip, and the results compared with the core's simulation outputs.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This product is available from Xilinx AllianceCORE partner, CAST, Inc. Please contact CAST, Inc. for pricing and additional information.

The C8051 core is licensed from Evatronix S.A.

Related Information

- CMOS single-chip 8-bit microcontrollers, Phillips, 1996.
- Addendum to the MCS®51 Microcontroller Family, Intel, 1996.
- 8-bit Embedded Controllers, Intel, 1990

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