UTOPIA Slave (CC143S)

February 22, 1999 | Product Specification

CoreEl MicroSystems

CoreEl MicroSystems

4046 Clipper Court
Fremont, CA 94538 USA
Phone: +1 510-770-2277
Fax: +1 510-770-2288
URL: www.coreel.com
E-mail: sales@coreel.com

Features

- Conforms to ATM Forum's Utopia Level 2 specifications, V 1.0
- Conforms to the cell transfer procedure required in ATM UNI devices
- Supports 8/16-bit Utopia operation
- Provides a 32-bit FIFO interface on the PHY side
- Supports a single port with configurable PHY address
- Supports SPHY operation in the Cell-Level Handshake
- Detects Runt cells on the Transmit side
- Drops excess bytes of a cell on the Transmit side
- Verifies parity on the Transmit side
- Indicates parity on the receive side
- HEC is always passed through
- Indicates occurrence of parity error(s) on the Transmit side
- Provides Overrun indication on Transmit side and Underrun indication on Receive side
- Statistics feature on the Receiver in the form of pulses for total cells and on the Transmitter in the form of pulses for total cells, excess cells, runt cells and parity error.

Applications

The UTOPIA core can be used in Asynchronous Transfer Mode (ATM) networking systems such as adapter cards, routers and switches.

AllianceCORE™ Facts

Core Specifics		
Supported Family	4000XL	Virtex
Device Tested	4013XL-08	V50-4
CLBs - Transmitter CLBs - Receiver	134 81	118[1] 80[1]
IOBs[2] - Transmitter IOBs[2] - Receiver	74 70	74 70
CLKIOBs - Transmitter CLKIOBs - Receiver	1 1	1 1
Performance	74 MHz[3]	79 MHz[3]
Xilinx Tools	M1.5i	M1.5i
Special Features	None	None

Provided with Core	
Documentation	Product Brief Datasheet Design Document Test Bench Design Document Test Scripts
Design File Formats	VHDL Compiled, EDIF netlist
Constraints File	Transmitter - txchip.ucf Receiver - rxchip.ucf
Verification	Script-based behavioral VHDL test bench, test vectors
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	Utopia Level 2 Specification V 1.0 from ATM Forum
Additional Items	None

Simulation Tool Used
Model Tech. V-system V 4.6f

Support
Support provided by CoreEl MicroSystems

Notes:
1. Utilization numbers for Virtex are in CLB slices.
2. Assuming all core I/O are routed off-chip.
3. Utopia Level 2, V1.0 specification requires only 50 MHz

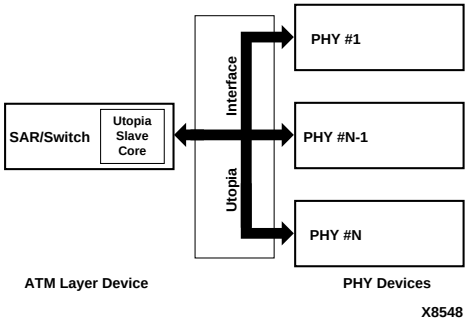

Figure 1: Data Transfer Between ATM Layer Device and UTOPIA Compatible PHY Devices

General Description

The CC143S CoreCell can be used in any Physical Layer Device (PHY) that performs the functions of Transmission Convergence sublayer. CC143S facilitates data transfer between the UNI (User Network Interface device) in ATM networks and a UTOPIA compatible ATM layer device as shown in Figure 1.

The UTOPIA Slave (CC143S) consists of two independent CoreCells for Transmitter and Receiver. It provides an interface to connect the PHY device to the ATM layer.

CC143S provides a facility to externally count the number of normal, runt, parity error and excess byte cells on the Transmitter side and the total number of cells on the Receiver side.

Functional Description

Transmitter

The Transmitter, CC143ST, provides an industry standard interface between the ATM layer and a PHY device through a 32 bit FIFO interface. It supports both SPHY and MPHY modes of operation, accepts cells from the ATM layer and writes them into the PHY Interface FIFO. It gives FIFO status on the txclav line. It detects selection of a port connected to the Transmitter by the ATM layer. The Transmitter detects and discards runt cells and excess bytes of a cell. It clubs the data received on the Utopia bus into 32 bits and sends it to the FIFO Interface. It also checks the parity on the txprty line, indicates occurrence of parity errors on parity_err_count_enb line, and generates the socin, eocin, datain_valid and discard_cell signals on the FIFO interface.

In the Transmit operation, data flows from ATM layer to Utopia interface. THe ATM layer controls the operation and provides an interface clock to the transmitter to synchronize all transfers.

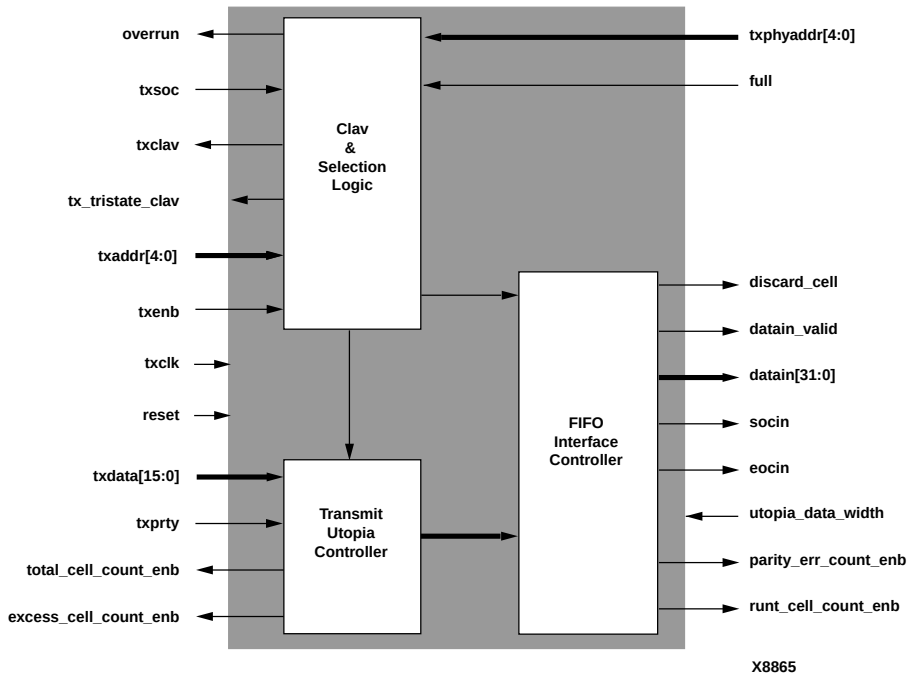

Figure 2: Slave CC143ST Block Diagram

The CC143ST is architecturally divided into the following blocks as shown in Figure 2. The operation of each block is described below.

Clav & Selection Logic

This block provides Clav status of the PHY port when its address is placed on the txaddr lines. The full status line of PHY ports is used to send the txclav status. The txphyaddr lines specify PHY port address.

The Selection Logic decides whether a PHY port connected to the CC143ST is selected by the ATM layer. It also decides whether it is a valid selection or not and hence avoids the possibility of an overrun condition.

Transmit Utopia Controller

This block monitors the handshake on the utopia bus. The txsoc and txprty lines indicate the Start of Cell and the odd parity of the data on the txdata bus respectively. The block calculates the parity and flags an error if it does not match the input parity. Pulses are generated on the statistical count lines to increment counters connected externally, if desired by the user. The txdata lines are configured for 16-bit or 8-bit operations with the utopia_data_width signal.

FIFO Interface Controller

This block receives data from the Transmit Utopia Controller block and converts it to the 32 bit FIFO interface width. It also validates the data sent to the FIFO through the datain_valid line. The start of a cell and end of cell to the FIFO is indicated by the socin line and eocin line respectively.

Receiver

The Receiver, CC143SR, accepts cells from a 32-bit FIFO interface and sends them to the ATM layer. It supports both SPHY and MPHY modes of operation. The Receiver reads data from the FIFO and splits it into Utopia compatible data width. It generates odd parity for data on txprty line, gives FIFO status on rx_clav line, and detects selection of a port connected to the Receiver by the ATM layer.

In the Receiver operation, data flows from Utopia interface to ATM layer. The ATM layer controls the operation and provides an interface clock to synchronize all transfers.

CC143SR is architecturally divided into the following blocks shown in Figure 3. The operation of each block is described below.

Clav and Selection Logic

This block is responsible for sending the Clav status of the addressed port to the Utopia interface. It is also responsible for the selection of FIFO from which data transfer to the Utopia side is to be made.

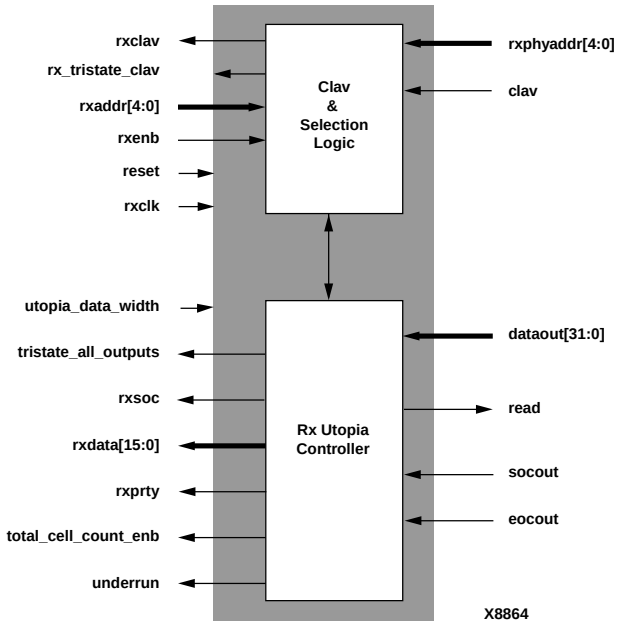

Figure 3: Slave CC143SR Block Diagram

The Clav indication and port selection are two entirely independent entities, operating in parallel.

Rx Utopia Controller

This block controls the data flow to Utopia. It sends data in the defined width format on the Utopia side. Start of Cell, synchronized with the first data transfer, is also sent. Cell count can be maintained on the Utopia side externally by the use of total_cell_count_enb signal that pulses high at the start of every cell transfer. This block provides an odd parity of data on the rxdata bus and indicates it on the rxprty.

Core Modifications

Normally, modifications are not possible by the user since the core is provided in a Xilinx netlist format. CoreEI can perform special modifications for additional charge. However, source code, where the customer can make modifications is available for an additional cost. Contact CoreEI Microsystems for more information.

Pinout

The pinout is not fixed to any specific device I/O. Signal names for transmitter and receiver UTOPIA blocks are provided in the block diagrams shown in Figures 2 and 3 and described in Tables 1 and 2, respectively.

Verification Methods

This core has been used in larger ASICs and is silicon proven. The FPGA verification was done by back annotating the implementation and simulating in a model technology V-System, V 4.6f, environment.

The testbench was written in VHDL with very powerful scripting capabilities and several scripts have been written for verifying the implementation. Additional tests can be added to the testbench by writing new scripts.

Recommended Design Experience

The following experience is recommended for the user to implement a complete design with CC143S:

- Familiarity with the FPGA architecture
- Familiarity with simulation, synthesis, and Xilinx tools
- Knowledge of the ATM and B-ISDN (Broadband ISDN) will be an added advantage

Table 1: Transmitter Utopia Block Signal Pinout

Signal	Signal Direction	Description
Transmitter Utopia Interface Signals		
txclk	Input	Transmit Utopia Clock.
txclav	Output	Active High. Indicates availability of space for complete cell in addressed FIFO.
tx_tristate_clav	Output	Active High Tristate. Enables txclav buffer when low.
txaddr[4:0]	Input	5-bit wide address driven from ATM layer to poll and select appropriate PHY device. txaddr[4] is MSB.
txenb	Input	Enable. Active low signal, validates data on txdata lines.
txdata[15:0]	Input	16-bit Utopia data bus driven from ATM to PHY. txdata[15] is MSB, txdata[0] is LSB in 16-bit data path.
txsoc	Input	Start of Cell. Active high signal indicates start of new cell.
txprty	Input	Data Path Parity. txprty serves as odd parity bit over txdata [7:0] in 8-bit mode and as odd parity bit over txdata [15:0] in 16-bit mode.
Transmit FIFO Interface Signals		
full	Input	Active High. Indicates that Cell FIFO is not ready to accept complete cell.
datain[31:0]	Output	32-bit data bus to Transmit PHY layer Cell FIFO.
datain_valid	Output	Active High signal. Validates data on datain bus.
socin	Output	Pulse High Synchronous with first data transfer to FIFO.
eocin	Output	Pulse high synchronous with last data transfer to FIFO.
discard_cell	Output	Active High. Pulses high upon reception of either parity error cell or runt cell on last FIFO-side data transfer.
Statistics Signals		
runt_cell_count_enb	Output	Pulses high when a runt cell is detected
parity_err_count_enb	Output	Pulses high when a parity error is detected during cell transmission

Table 1: Transmitter Utopia Block Signal Pinout (Cont)

Signal	Signal Direction	Description
total_cell_count_enb	Output	Pulses high when a Start Of Cell is detected
excess_cell_count_enb	Output	Pulses high when an excess byte cell is detected
overrun	Output	Active high. When high indicates that the ATM layer is selecting a PHY port whose FIFO is full.
Configuration Signals		
txphyaddr[4:0]	Input	5-bit Physical Port Address
utopia_data_width	Input	Data width configuration signal for the Utopia side data bus. '1' indicates a 16-bit bus, '0' indicates an 8-bit bus - txdata[7:0].
reset	Input	Active high asynchronous reset

Available Support Products

The support tools or related products that are available to help the user to integrate the CoreCell are listed below. These products must be purchased separately.

- Utopia Slave test bench
- Utopia Master CoreCell
- Utopia Master test bench

Ordering Information

For information on this or other products mentioned in this specification, contact CoreEl MicroSystems directly from the information provided on the front page.

Related Information

RFC documents can be downloaded from several websites, including:

sunsite.auc.dk/RFC/
ftp.digital.com/pub/net/info/RFC/ds.internic.net/rfc/

Table 2: Receiver Utopia Block Signal Pinout

Signal	Signal Direction	Description
Receiver Utopia Interface Signals		
rxclk	Input	Receive Utopia Clock.
rxclav	Output	Active High. Indicates availability of complete cell in addressed FIFO.
rx_tristate_clav	Output	Active high tristate. Enables rxclav buffer when low.
rxaddr[4:0]	Input	Utopia bus address lines.
rxenb	Input	Active low. Controls data flow from PHY to ATM layer.
rxsoc	Output	Active High. Indicates start of data transmission cell.
rxdata[15:0]	Output	16-bit Utopia Data Bus.
rxprty	Output	Sends parity bit for current word/byte being sent to ATM side. Indicates odd parity for data on rxdata bus.
tristate_all_outputs	Output	Active High Tristate. When low, rxsoc, rxdata, and rxprty signal buffers are enabled.
FIFO Interface Signals		
clav	Input	Active High. Indicates availability of complete FIFO cell.
dataout[31:0]	Input	32-bit data lines: carry data from FIFO to CC143SR.
read	Output	Active High. Is the read enable signal to the FIFO connected.
socout	Input	Active high. Indicates start of FIFO cell transfer.
rxphyaddr [4:0]	Input	5-bit Physical Port Address.
eocout	Input	Active High. Indicates end of FIFO cell transfer.
Statistics Signals		
totalcell_count_enb	Output	Active High. Pulses high upon start of cell transfer.
underrun	Output	Active High: indicates that ATM layer is selecting a PHY port with empty FIFO.
Configuration Signals		
reset	Input	Active High. Asynchronous reset.
utopia_data_width	Input	Data width configuration signal for the Utopia side data bus. '1' indicates a 16-wide bus, '0' indicates an 8-bit bus -rxdata[7:0].

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm