Deltatec

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Features

- SMPTE/EBU LTC time code generator
- Lock-on external (video) reference
- PAL/NTSC support
- 27 Mhz clock input for internal timing
- Five 16-bit double buffered registers for time code data and sync word
- Versatile synchronization

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core data sheet
Design File Formats	XNF/Edif netlist
Constraints File	.ucf
Verification	VHDL testbench, Simulation vector
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	Application note, Sample design
Additional Items	None
Simulation Tool Used	
1076 Compliant VHDL Simulator	
Support	
Support provided by Deltatec	

Applications

The LTC generator core is used in video distribution/editing equipment.

Table 1: Core Implementation Data

Supported Family	Device Tested	CLBs[2]	Clock IOBs	IOBs[1]	Performance (MHz)	Xilinx Tools	Special Features
Virtex	V100-4	69	2	27	85	M2.1i	Distributed DPRAM
XC4000XLA	4013XLA-07	60	2	27	71	M2.1i	Distributed DPRAM

Notes:
1. Assuming all core I/Os are routed off-chip
2. Utilization numbers for Virtex are in CLB slices.

General Description

The LTC generator core accepts 80 bits of SMPTE/EBU audio Longitudinal Time Code from its 16 bits wide µP interface.

The LTC generator synchronizes on the falling edge of the incoming reference signal to start transmission of the received time code.

The 80-bit long time code is serialized, bi-phase mark encoded, and transmitted over the full video frame.

A simple external analog audio interface is necessary to properly shape (gain & slope adjustment) the digital LTC bitstream. See the application note.

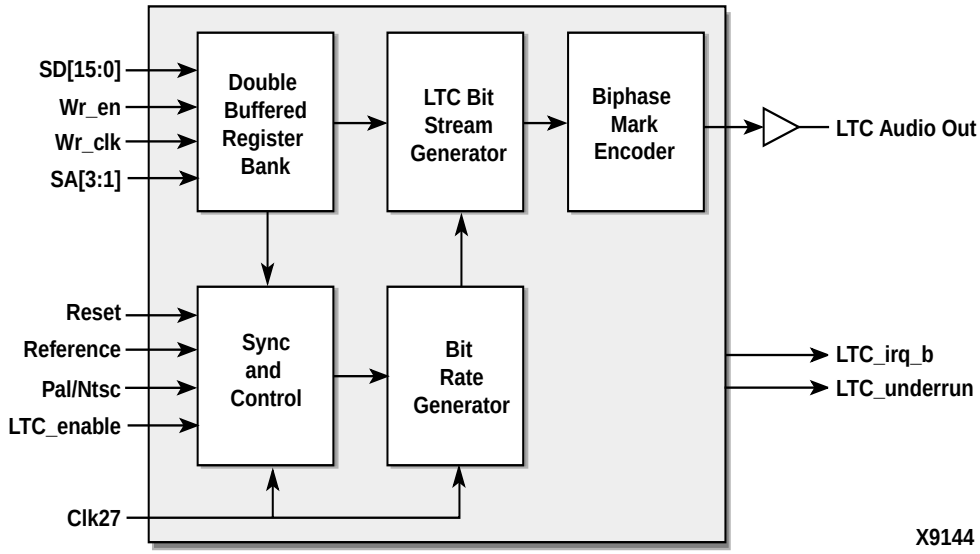

Figure 1: LTC Generator Block Diagram

Functional Description

From the µP point of view, the LTC generator appears as five 16-bit write-only registers holding the 80-bit time code data formatted as in table 2. The µP is responsible to upgrade this data at each frame.

For basic applications, only the frames, seconds, minutes, and hours units & tenths must be incremented at each video frame; and the phase correction bit (27 for NTSC, 59 for PAL) must be adjusted so that the full 80-bit LTC word contains an even number of zeros, while with the exception of the constant 0xBFFC sync word, all other bits are null.

For a detailed LTC bits description, see the relevant normative references.

A high to low transition on the input reference signal starts transmission of the next LTC. Typically this reference is driven by the video field parity (odd/even).

The LTC word must begin in line 7 (+- 1 line) in fields 1 & 3 for NTSC, and line 2 (+- 1 line) in fields 1 & 3 & 5 & 7 for PAL and occupies the full frame. Proper alignment of the reference against the video timing must be provided by the user.

A five-16-bit, double-buffered register set is used so the µP can update the next timecode data while transmission of the current one proceeds.

Two handshake signals are generated:

- LTC_irq_b is an active low interrupt request pulse signalling the µP that a new data set can be loaded.
- LTC_underrun is an active high status signalling that no new LTC data was available at the frame end. Bring Reset high or LTC_enable low to reset this status.

Sync word register write is used to the signal, New Data Set Ready for handshaking and must occur after all other registers update.

The µP registers interface can be

- Synchronous: Wr_clk is the free-running µP clock, Wr_en controls register write operations.
- Asynchronous: Wr_clk is the asynchronous µP write control (active on rising edge), Wr_en can either be tied high or used as Chip Select (active high).

Table 2: LTC Generator Register Map

Byte Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Binary Group 4				11	10	Frames tens		Binary Group 1				Frames units			
2	Binary Group 5				27	Seconds tens			Binary Group 2				Seconds units			
4	Binary Group 6				43	Minutes tens			Binary Group 3				Minutes units			
6	Binary Group 7				59	58	Hours tens		Binary Group 4				Hours units			
8	Synchronization word: 0xBFFC															

Pinout

For easy integration with user design/device, no fixed pinout is required. A sample implementation will provide an example pinout. Signal names are shown in the block diagram in Figure 1 and described in Table 3.

Table 3: Core Signal Pinout

Signal	Signal Direction	Description
SD[15:0]	Input	µP data bus
Wr_en	Input	µP write enable
Wr_clk	Input	µP write clock
SA[3:1]	Input	MP address
Reset	Input	Asynchronous reset
Reference	Input	LTC frame start reference (falling edge)
Pal/Ntsc	Input	PAL (1)/NTSC (0) standard select
LTC_enable	Input	LTC enable: when set to 1, LTC transmission begins at next frame
Clk27	Input	27 Mhz video clock
LTC_audio_out	Output	Digital LTC output
LTC_irq_b	Output	LTC interrupt output
LTC_underrun	Input	LTC underrun status

Please contact Deltatec directly for any required modifications.

Core Modifications

Customization of the core (8 bit µP interface for example) can be performed by Deltatec to perfectly match the user's needs.

Core Assumptions

- The bi-directional data bus has been split into two separate buses: DIN[7:0] and DO[7:0]
- The 1.5 stop bit mode (for 5 bit word length) is not supported
- Signals rd2, wr2, xin and xout have been eliminated from the interface

Verification Methods

VHDL functional and timing simulation have been performed on the core; VHDL testbench and simulation vectors for the sample design are provided.

Recommended Design Experience

The user must be familiar with VHDL/Verilog synthesis/simulation and Xilinx design flows.

Ordering Information

This product is available from Deltatec. Please contact Deltatec for additional information and pricing.

Related Information

SMPTE 12M-1995 Television, Audio and Film–Time and Control Code
IEC 461-1986 Time and Control Code for Video Tape recorders

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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