

## Dolphin Integration

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## Features

- Full binary code compatibility with the original 8051/52
- Single cycle instruction execution for most of the opcodes. On average 8 times over the performance (in terms of MIPS) of the standard 8051/52 at the same clock frequency
- Some instructions up to 12x standard 8051/52
- De-multiplexed Address/Data Bus to allow easy connection to memory
- Dedicated hardware to accelerate multiply and division instructions
- 2 Data Pointers for faster memory copies and indexing
- The I/O ports (P0, P1, P2, P3) and the alternate functions like external interrupts are separated, providing extra port pins when compared with the standard 8051/52
- Extra bus for easy integration of extra peripherals and Special Function Registers
- Up to 6 external interrupts plus a software interrupt (Trap instruction)

AllianceCORE™ Facts	
<b>Core Specifics</b>	
See Table 1	
<b>Provided with Core</b>	
Documentation	Specification Manual; User Guide
Design File Formats	EDIF netlist, NCD netlist, VHDL source available extra
Constraints File	xflip52.ucf
Verification	Test vectors, VHDL testbench available extra
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	User Guide
Additional Items	Bus Monitor behavioral model
<b>Simulation Tool Used</b>	
ModelSim	
<b>Support</b>	
Support provided by Dolphin Integration	

Notes:

1. Assuming all core I/Os are routed off-chip.
- Extra dedicated output bus (Bus Monitor) for real time trace disassembly of the code execution, easing hardware/software co-verification
  - Static synchronous design with no internal tri-states

## Applications

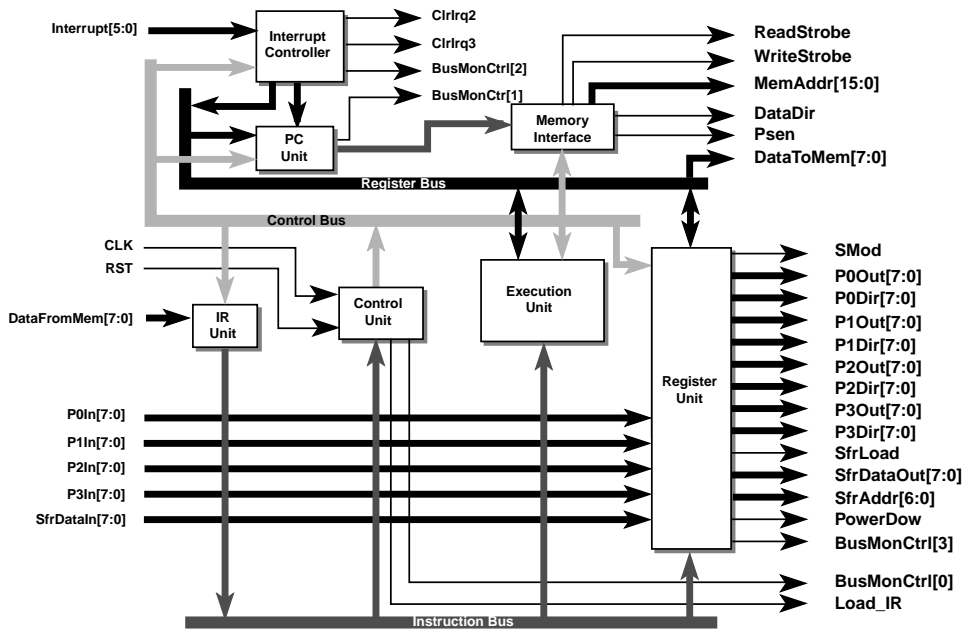
- 8-bit data processing applications
- Low power consumption applications
- Complex processing applications
- High speed applications

**Table 1: Core Implementation Data**

Supported Family	Device Tested	CLB Slices	Clock IOBs <sup>1</sup>	IOBs	Performance (MHz)	Xilinx Tools	Special Features
Spartan-II	2S150-6	1174	1	172	19.6 <sup>2</sup>	M2.1i	SelectRAM
Virtex-E	V300E-8	1184	1	172	27.7 <sup>2</sup>	M2.1i	SelectRAM
Virtex	V300-6	1015	1	172	29.8	M1.5i	SelectRAM

Notes:

1. Assuming all core I/Os are routed off-chip
2. Preliminary performance. Contact Dolphin Integration for the latest numbers



X9006

Figure 1: Flip8051-PR Block Diagram

## General Description

The Flip8051-PR core is an enhanced version of the 8051/52 microprocessor (peripherals, such as Timers and Serial Interface, are not included). It is 100% code compatible with the original 8051/52 and uses modern processor techniques to increase processing speed an average of eight times while running at the same clock frequency. The extra processing power can be used to perform high speed applications, or to run the same software at a slower clock speed, for saving power consumption, or even to increase the complexity of your 8051/52 based application.

## Functional Description

The Flip8051-PR is partitioned into modules as shown in Figure 1.

### IR Unit

Block that stores the current instruction and its operands.

### Control Unit

This block is the main state machine of the processor. It generates the control signals depending on the state of the machine and the current instruction loaded in the IR Unit.

### Execution Unit

It performs 8 bit arithmetic and logical operations. It includes an ALU unit, a Boolean operation unit and a Multiply/Division unit to speed up the execution time. It can also perform single bit manipulation.

### Register Unit

This block contains the internal data memory divided into 3 blocks as in the original 8051/52. These are the Lower 128 bytes (direct/indirect addressing), Upper 128 bytes (indirect addressing) and SFR space (direct addressing). The lower and upper bytes are implemented in distributed RAM while SFR space is implemented in flip-flops.

The Lower 128 bytes as in the original 8051/52 can be divided into 3 segments:

- Four 8-bit register banks, addresses 00h to 1fh
- Bit addressable area, addresses 20h to 2Fh
- Free user area, addresses 30h to 7Fh

The Upper 128 bytes are free user as in the standard 8051/52.

The SFR space, contains the same registers as the original 8051/52 with the exception of the registers used for the timers and the serial interface.

Through the extra SFR bus it is possible for the user to map extra SFR registers to the SFR space to control user's hardware.

## PC Unit

It implements the Program Counter that provides the addresses of the instruction and data to be fetched.

## Memory Interface

This block interfaces with Program and Data Memory, generating the read/write strobes and fetching instructions and data from the address specified in the PC Unit.

## Interrupt Controller

Block that manages up to 6 external interrupts. The interrupt control unit determines whether an interrupt should be granted or not and when it will be granted. It also provides the vector address of the corresponding interrupt to the PC Unit.

External interrupts 0 and 1, are user configurable as in the original 8051/52 (level or edge triggered).

## Core Modifications

Additional parts of the system may be developed by Dolphin, according to the user's application. Typically, Dolphin can supply the Flip8051-PR core with compatible standard 8051 peripherals (Timers and Serial Interface). These peripherals are available as VHDL, EDIF or NCD netlists (Flip8051-CR). The three main configurations are:

- Flip8051-PR: Core without any peripheral
- Flip8051-CR: Flip8051-PR with 2 timers and a serial interface
- Flip8052-CR: Flip8051-PR with 3 timers and a serial interface

On request, Dolphin Integration can also provide the Flip8051-PR/CR core with any peripheral the customer may need for his 8051/52 based application. Contact Dolphin directly to discuss any specific requirements.

## Pinout

Signal names are provided in the block diagram shown in Figure 1, and described in Table 1.

## Core Assumptions

The Flip8051-PR has an externally accessible Special Function Register (SFR) bus. This allows easy integration of extra registers controlling user's peripherals, into the SFR address space of the Flip8051-PR.

**Table 2: Core Signal Pinout**

Signal	Signal Direction	Description
<b>System Signals</b>		
RST	Input	Asynchronous active high reset. Signal synchronized to the system clock.
CLK	Input	System clock.
PowerDown	Output	High when processor is in Power Down state.
<b>Memory Interface</b>		
DataFromMem[7:0]	Input	External memory data bus in.
DataToMem[7:0]	Output	External memory data bus out.
DataDir	Output	Direction of external memory data bus. High when an input, low when an output.
MemAddr[15:0]	Output	External Address bus to memory and Signal Direction.
Psen	Output	Low when accessing program space.
ReadStrobe	Output	Low when reading external memory.
WriteStrobe	Output	Low when writing external memory.
<b>Extended SFR</b>		
SfrDataIn[7:0]	Input	External special function register data bus in.
SfrDataOut[7:0]	Output	External special function register data bus out.
SfrAddr[6:0]	Output	External special function register address bus.
SfrLoad	Output	Synchronous signal, high to latch data into external special function register.
<b>Interrupts</b>		
Interrupt0	Input	When level-activated, active low interrupt 0. When transition activated, active on falling edge.

Table 2: Core Signal Pinout (Cont.)

Signal	Signal Direction	Description
Interrupt1	Input	When level-activated, active low interrupt 1. When transition activated, active on falling edge.
Interrupt2	Input	Active high interrupt 2. Can be used as a Timer 0 interrupt.
Interrupt3	Input	Active high interrupt 3. Can be used as a Timer 1 interrupt.
Interrupt4	Input	Active high interrupt 4. Can be used as a serial interrupt (transmit or receive).
Interrupt5	Input	Active high interrupt 5. Can be used as a Timer 2 interrupt.
ClrIrq2	Output	Hardware clear external interrupt request 2.
ClrIrq3	Output	Hardware clear external interrupt request 3.
<b>Signal Ports</b>		
P0In[7:0]	Input	Port 0 input bus.
P0Out[7:0]	Output	Port 0 output bus.
P0Dir[7:0]	Output	Port 0 direction bus.
P1In[7:0]	Input	Port 1 input bus.
P1Out[7:0]	Output	Port 1 output bus.
P1Dir[7:0]	Output	Port 1 direction bus.
P2In[7:0]	Input	Port 2 input bus.
P2Out[7:0]	Output	Port 2 output bus.
P2Dir[7:0]	Output	Port 2 direction bus.
P3In[7:0]	Input	Port 3 input bus.
P3Out[7:0]	Output	Port 3 output bus.
P3Dir[7:0]	Output	Port 3 direction bus.
<b>Special Pins</b>		
Load_IR	Output	Only for Serial Interface when connected. Used for data synchronization
SMod	Output	Only for Serial Interface when connected. Configuration bit to fix baud rate of serial interface.

Table 2: Core Signal Pinout (Cont.)

Signal	Signal Direction	Description
<b>Pins For Test</b>		
BusMonCtrl[3]	Output	When high, indicates that there is an Idle Mode request.
BusMonCtrl[2]	Output	When high, indicates an IRQ accepted.
BusMonCtrl[1]	Output	When high, indicates a data is fetching into the instruction queue and the Program Counter is going to change.
BusMonCtrl[0]	Output	When high, indicates the start of a new instruction execution in the next clock cycle.

The Flip8051-PR is provided with 6 external interrupt pins. The Flip8051-PR separates out external interrupts from the I/O ports allowing real 32 bits of general purpose I/O.

It is possible to connect the signals PjIn, PjOut and PjDir (where j=0,1,2,3) to bi-directional pads to obtain an I/O port. The I/O port signal direction PjDir is controlled by an extra Special Function Register called Pj\_Dir. Pj\_Dir registers are located at addresses 0xA4, 0xA5, 0xA6, and 0xA7. When bit i of Pj\_Dir is set to '1', bit i of Pj is used as input (PjIn[i]), otherwise bit i of Pj is used as output (PjOut[i]).

The Flip8051-PR has 2 Data Pointers for faster indexing and copying. An extra SFR register, DPSEL (Data Pointer Select), is implemented to swap from one Data Pointer to the other one. It is located at address 0x92.

In the original 8051/52, operation code A5 is not used. The Flip8051-PR uses it as a trap instruction to give to the user the possibility of incorporating a software interrupt.

## Verification Methods

The Flip8051-PR has been tested in simulation using a test bench that consists of a self-checking assembly program (Intel hex format object file). The simulation environment and minimal test vectors for verifying the functionality are supplied with the core. The full virtual testbench can be delivered as a separate option.

Other tests have been performed, most of which are carried from the acceptance procedures performed by our customers.

Using the supplied Bus Monitor Behavioral Model, any execution of a program running on the Flip8051-PR can be verified in the simulation environment.

An Evaluation Board, using the Xilinx device, provides the customer with an easy method for verifying and debugging software based on Flip8051-PR.

## Recommended Design Experience

Users should be familiar with 8051/52 microcontrollers, skilled in assembly and/or C language.

## Available Support Products

As the Flip8051-PR is 100% code compatible with the standard 8051/52, any tool that runs on the 8051/52 can run on the Flip8051-PR. Any 8051/52 assembler/C compilers and debuggers can be also used.

Note: Since the execution time in the Flip8051-PR is about 8 times faster than the standard 8051/52, our In-design Evaluation Board will be the most convenient tool for emulating Flip8051-PR-based software. You can use third party emulators, taking into account that tasks carried out in the assembly program rely on program execution speed.

## Ordering Information

The Flip8051-PR core is provided under license from Dolphin Integration for use in Xilinx devices in EDIF or NCD netlists. VHDL source is available for additional cost. Please, contact Dolphin Integration for more information on this or other Dolphin products.

## Related Information

### Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.  
2100 Logic Drive  
San Jose, CA 95124  
Phone: +1 408-559-7778  
Fax: +1 408-559-7114  
URL: [www.xilinx.com](http://www.xilinx.com)

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)  
+1 408-879-5017 (outside the US)  
E-mail: [literature@xilinx.com](mailto:literature@xilinx.com)

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381  
E-mail: [alliancecore@xilinx.com](mailto:alliancecore@xilinx.com)  
URL: [www.xilinx.com/products/logiccore/alliance/tblpart.htm](http://www.xilinx.com/products/logiccore/alliance/tblpart.htm)



## Flip8051-PR Request Form

To: **Dolphin Integration**  
 FAX: **+33 4 76 90 29 65**  
 E-mail: **flip@dolphin.fr**

Dolphin Integration ships Xilinx netlist versions of the Flip8051-PR core customized to your specification. Please, fill out and fax this form so that Dolphin Integration can respond with an appropriate quotation for the target Xilinx FPGA.

From: \_\_\_\_\_  
 Company: \_\_\_\_\_  
 Name: \_\_\_\_\_  
 Address: \_\_\_\_\_  
 Country: \_\_\_\_\_  
 Phone: \_\_\_\_\_  
 Fax: \_\_\_\_\_  
 E-mail: \_\_\_\_\_

### Implementation Issues

**1. Do you intend to add peripherals to the Flip8051-PR:**

\_\_\_\_\_ Yes  
 \_\_\_\_\_ No

**2. Which configuration out of the three main configurations is required:**

\_\_\_\_\_ Flip8051-PR  
 \_\_\_\_\_ Flip8051-CR  
 \_\_\_\_\_ Flip8052-CR

**3. In addition to this configuration, which standard peripherals are required? Specify:**

\_\_\_\_\_ Number of timers (1, 2 or 3)  
 \_\_\_\_\_ Serial Interface

**4. Do you need other peripherals? Specify:**

**5. Please specify any additional requirements:**

### Business Issues

**6. Indicate timescale of requirements:**

Date for decision \_\_\_\_\_  
 Date for planning \_\_\_\_\_  
 Required delivery date \_\_\_\_\_

**7. Indicate your area of responsibility:**

\_\_\_\_\_ Decision maker  
 \_\_\_\_\_ Budget holder  
 \_\_\_\_\_ Recommender

**8. Has a budget been allocated for the purchase?**

\_\_\_\_\_ Yes  
 \_\_\_\_\_ No

**9. What volume do you expect to ship of the product using this core? \_\_\_\_\_**

**10. What major factors will influence your decision?**

\_\_\_\_\_ Cost  
 \_\_\_\_\_ Customization  
 \_\_\_\_\_ Testing  
 \_\_\_\_\_ Implementation size

**11. Are you considering any other solutions?**