EP100 PowerPC Bus Slave

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Features

- Supports Virtex™, Virtex-E™, and Spartan™-II FPGAs
- Fully supports PowerPC™ 60x bus protocol including PowerPC 603, 604, 740, 750 and MPC8260
- Direct support for standard asynchronous SRAM with programmable (source code version) wait states and synchronous BURST SRAM
- Burst access support using conventional asynchronous SRAM
- Programmable (source code version) base address and address range for all the back-end interfaces
- Additional back-end bus interface support for on-chip and off-chip logic and register access
- Back-end bus interface supports user device with various wait states
- Burst access support on back-end bus interface which utilizes a post write buffer
- Processes the memory requests on the PowerPC bus
- Handles separate address and data bus tenure to support address pipelining
- Supports PowerPC bus address only transfer mode
- Supports address retry generated by an external device
- Issues address retry to the new bus request when the post-write buffer is still waiting for the back-end bus to retrieve the data

AllianceCORE™ Facts

Core Specifics	
Supported Family	Virtex-E
Device Tested	V400E-8
CLB Slices	475
Clock IOBs[1]	1
IOBs[1]	330
Performance (MHz)	80
Xilinx Tools	3.2i
Special Features	None
Provided with Core	
Documentation	User guide
Design File Formats	EDIF netlist
Constraints File	Top201.ucf
Verification	VHDL or Verilog test bench
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	None
Additional Items	None
Simulation Tool Used	
Model Technology Modelsim™ 5.4b	
Support	
Support provided by Eureka Technology	

Notes:
1. Assuming all core I/Os are routed off-chip

Applications

The PowerPC bus slave is used in a wide variety of fields. The following are just a few examples:

- Defense
- Medical
- Communication
- Any peripheral device using a PowerPC microprocessor

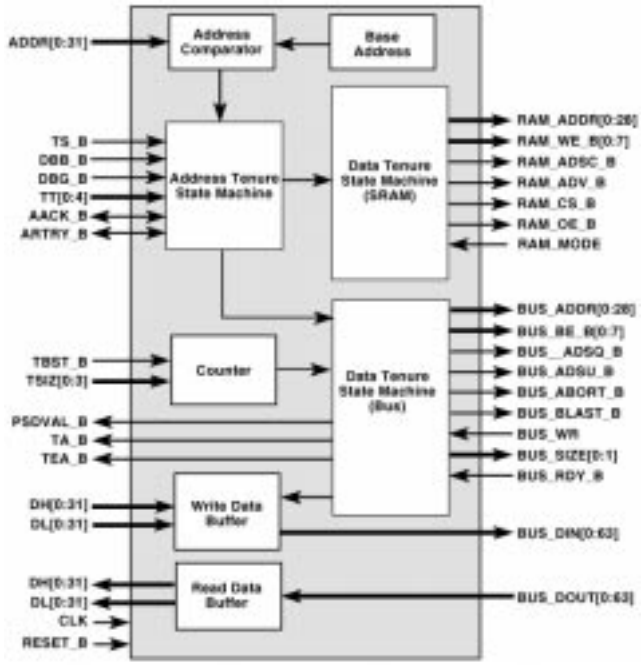

Figure 1: EP100 PowerPC Bus Slave Block Diagram

General Description

The PowerPC bus slave device is a bus interface unit designed for the PowerPC host bus. It is designed to work with any 60x or MPC8260 compliant bus architecture.

It has two user interfaces; one for interfacing with on-chip and off-chip user logic and register and the second interface is a direct interface to external asynchronous SRAM and synchronous BURST SRAM.

Both burst and single beat data transfer are supported on the SRAM and back-end bus interfaces. Each interface has its own set of programmable base address and address range.

For asynchronous SRAM, the number of wait states can be programmed from zero to seven, depending on the user's need.

For back-end bus interface, a post write buffer is used for better performance. In either read or write transaction, the back-end bus interface can handle different wait states inserted by the user device.

The PowerPC bus slave supports advance features of the PowerPC bus including address pipelining, address retry, address only transfer mode and separate address and data bus tenure to improve bus performance.

Functional Description

The PowerPC slave device provides an efficient interface for SRAM or on-chip and off-chip user logic and registers. It translates the complex address and data tenure of the PowerPC host bus to simple user interface. The following is a brief description of each individual block with respect to Figure 1.

Address Comparator

The incoming address is compared with the base address for the SRAM and backend bus. This information will pass to the Address Tenure State Machine.

Address Tenure State Machine

A read/write access through the slave device from PowerPC bus is indicated by the assertion of the TS_B signal to the Address Tenure State Machine. If the access location falls within the memory range of the SRAM/backend bus, the Address Tenure State Machine will be triggered and the information will pass to the Data Tenure State Machine. The state machine will return to the idle state one cycle after ARTRY_B.

Counter

The Counter is used to decode the transfer size based on TBST_B and TSIZ[3:0] which are received from the PowerPC bus. It helps the Data Tenure State Machine (Bus) to determine the end of the data transfer.

Write Data Buffer

The post Write Data Buffer is exclusively used for backend bus for better performance. It supports zero wait state data transfer on the PowerPC bus. Moreover, it allows the slave to serve the SRAM access while the backend bus retrieves the data from the write buffer. The slave device will assert ARTRY_B to the new backend bus request when the write buffer is still busy serving the current backend bus write transaction.

Read Data Buffer

The Read Data Buffer is exclusively used for backend bus for fast Tco. The read data from the backend bus are first stored in this buffer before going out to the PowerPC bus.

Base Address

The base address for SRAM and the backend bus is hardwired to the user's specification. This is used for address comparison.

SRAM/Bus Data Tenure State Machine

Depending on the address range, either the SRAM or the backend bus Data Tenure State Machine receives the information from the Address Tenure State Machine, it will then wait for DBG_B and DBB_B and start the data transfer. The state machine will go back to the idle state when the data transfer is completed.

Core Modifications

The PowerPC bus slave is designed in the XCV400EFG676 FPGA. Cores for other packages can also be supported. Eureka Technology will contract to modify the core to your specifications. Most of the data widths are parameterizable; contact Eureka Technology for customization.

Verification Methods

Functional simulation has been done using Model Technology ModelsimTM 5.4b. Static timing analysis has been done for all paths using the timing analyzer in Xilinx Foundation Series 3.2i.

Pinout

The pinout of the EP100 core has not been fixed to specific FPGA I/O, thereby allowing flexibility with a user's application. Signal names are shown in Figure 1 and described in Table 2.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
ADDR[0:31]	Input	PowerPC address bus
TS_B	Input	Transfer start
DBB_B	Input	Data bus busy
DBG_B	Input	Data bus grant
TT[0:4]	Input	Transfer type
AACK_B	Input/output	Address acknowledge
ARTRY_B	Input/Output	Address retry
TBST_B	Input	Transfer burst
TSIZ[0:3]	Input	Transfer size
PSDVAL_B	Output	Partial data valid
TA_B	Output	Transfer acknowledge
TEA_B	Output	Transfer error acknowledge
DH[0:31]	Input/output	Data bus high
DL[0:31]	Input/output	Data bus low
CLK	Input	System clock
RESET_B	Input	System reset
RAM_ADDR[0:28]	Output	SRAM address
RAM_WE_B[0:7]	Output	SRAM write enable
RAM_ADSC_B	Output	Burst SRAM address strobe
RAM_ADV_B	Output	Burst SRAM address advance
RAM_CS_B	Output	SRAM chip select
RAM_OE_B	Output	SRAM output enable
RAM_MODE	Input	SRAM mode select
BUS_ADDR[0:28]	Output	Backend bus address
BUS_ADSQ_B	Output	Qualified bus start
BUS_BE_B[0:7	Output	Bus byte enable
BUS_ADSU_B	Output	Unqualified bus start
BUS_ABORT_B	Output	Backend bus abort
BUS_BLAST_B	Output	Last burst bus data
BUS_WR	Output	Bus write/read
BUS_SIZE[0:1]	Output	Bus transfer size
BUS_RDY_B	Input	Bus ready
BUS_DIN[0:63]	Input	Bus input data
BUS_DOUT[0:63]	Output	Bus output data

Recommended Design Experience

Users should decide the target device and there is no requirement in using the PowerPC bus slave core.

Ordering Information

If you have inquiries or want to license our core, please contact Eureka Technology directly. Eureka Technology retains the right to make changes to these specifications at any time without notice.

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Related Information

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