GVA-200A DSP Hardware Accelerator

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Product Specification

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Features

- 40 MHz maximum input A/D sample rate
- 15 MHz sample Bandwidth
- FPGA Logic Expansion (from 13K to 62K gates)
- Dedicated 64K X 16 SRAM for each FPGA
- 40 bit FPGA Local Bus with External Data Access
- Xilinx FPGA Master Parallel, Master Serial and Download Cable Configurations
- 80 MHz maximum output D/A sample rate
- Stereo Audio Amplifier with Stereo Jack
- Separate FPGA Power Plane for Power Measurement
- External 3.3V Jack for High Current FPGAs
- Programmable A/D Sample Clock
- External High Stability Clock Input
- Supports New Xilinx Spartan Family of FPGAs

General Description

The GVA-200 Digital Signal Processing Hardware Accelerator is designed for the implementation of complex DSP or other channel coding designs. This platform provides a highly flexible environment for the integration of various software and hardware DSP applications using the Xilinx XC4000XL and Spartan families.

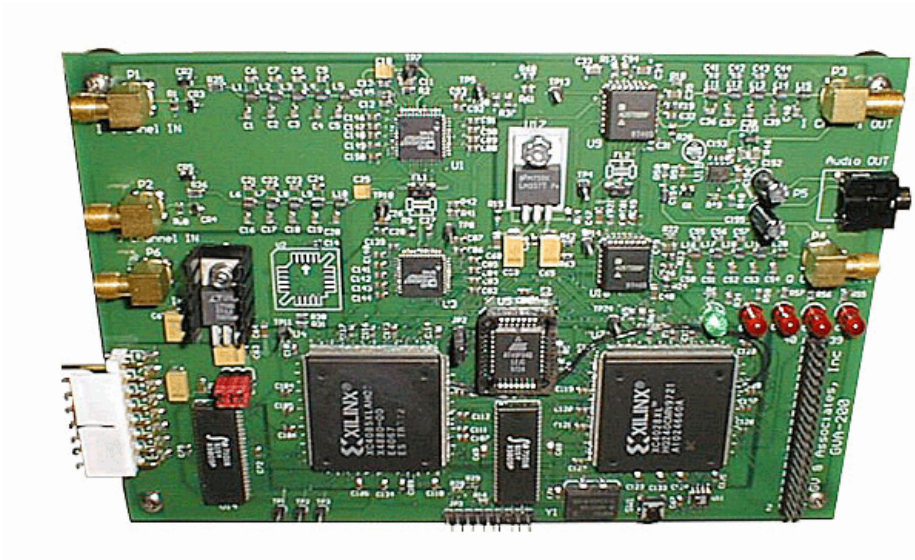

Figure 1: GVA-200A DSP Hardware Accelerator

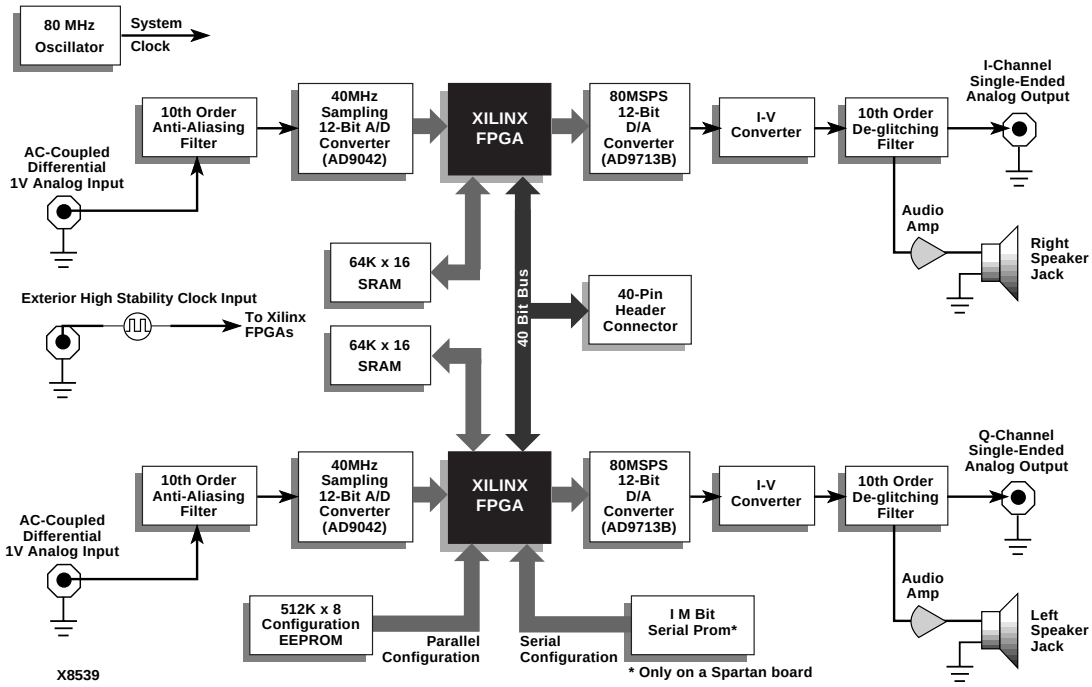

Figure 2: GVA-200A Block Diagram

The GVA-200 supports the following Xilinx FPGAs:

- XC4013XL-3PQ240C
- XC4020XL-3HQ240C
- XC4028XL-3HQ240C
- XC4036XL-3HQ240C
- XC4044XL-3HQ240C
- XC4052XL-3HQ240C
- XC4062XL-3HQ240C
- XC4085XLA-3HQ240C
- XCS30XL-3PQ240C
- XCS40XL-3PQ240C
- XCS30-3PQ240C
- XCS40-3PQ240C

Functional Description

The platform's general configuration consists of an I and Q channel which is passed through a 10^{th} order low pass filter. The 10^{th} order low pass filter band limits the input signals to a 15 MHz bandwidth. The signal rejection is -60 dB at 25 MHz. Next, the signals are digitized by a 12 bit A/D. The sample rate (maximum of 40 MHz) of the A/D is programmable since it is generated by the Xilinx FPGA. The digitized signals are then ready to be processed by the customer's algorithm that is implemented in hardware by the Xilinx FPGA.

Once the signals have been processed, a 80 MSPS D/A (via the Xilinx FPGA) converts them back to an analog waveform. The processed data may also be sent to the external 40-bit data port. The processed analog waveforms are passed through a 10^{th} order smoothing filter which is band limited to 15 MHz. The filtered analog signal is connected to a 50 ohm BNC output for viewing and to an audio amp that may be accessed via the stereo jack.

Each Xilinx FPGA has access to a 64K x 16 Static RAM that can be used for temporary data storage. The Xilinx FPGA may also access unused address space in the configuration EPROM. Also, the two Xilinx FPGAs have a 40 bit local bus for direct transfer of data between the two devices. This local bus can be configured as an interface to a TMS320C31, TMS320C40 or other Digital Signal Processor. For non-specific clock requirements, an external clock source is available.

The GVA-200 Digital Signal Processing Hardware Accelerator also supports the new Xilinx XLA and Spartan Family of FPGAs.

Ordering Information

This product is available directly from GV & Associates. Please contact them for pricing and more information.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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