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Features

- Supports Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- Supports, G.721, G.723, G.726, G.726a, and G.727, G.727a ITU standards
- 8 channel duplex encoding and decoding
- Online configurable for different compression rates, µ-law and A-law for each encoding or decoding channel
- A generic parameter in VHDL RTL version
- Coding (encode or decode) for one data sample in 16 clock cycles (min)
- Can work in both burst and continuous modes
- Multiplication mapped onto a single multiplier for compact implementation
- Conforms fully to ITU test vectors

Applications

- Digital Enhanced Cordless Telecommunications (DECT)
- Video conferencing
- Telecommunications

AllianceCORE™ Facts

Core Specifics	
Supported Family	Virtex
Device Tested	V150-6
CLBs	1530
Clock IOBs	1
IOBs[1]	44[2]
Performance	16 MHz
Xilinx Tools	M1.5i
Special Features	Distributed RAM
Provided with Core	
Documentation	User Guide, Design Guide
Design File Formats	EDIF netlist, VHDL RTL available extra
Constraints File	xpcmcod_pads.ucf
Verification	Testbench, Test Vectors
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	None
Additional Items	Bit-accurate C model
Simulation Tool Used	
Synopsys VSS, ModelSim	
Support	
Support provided by ISS	

Note:
1. Assumming all core I/0s are routed off-chip
2. Using PCM coding, S and SD are 8-bit wide

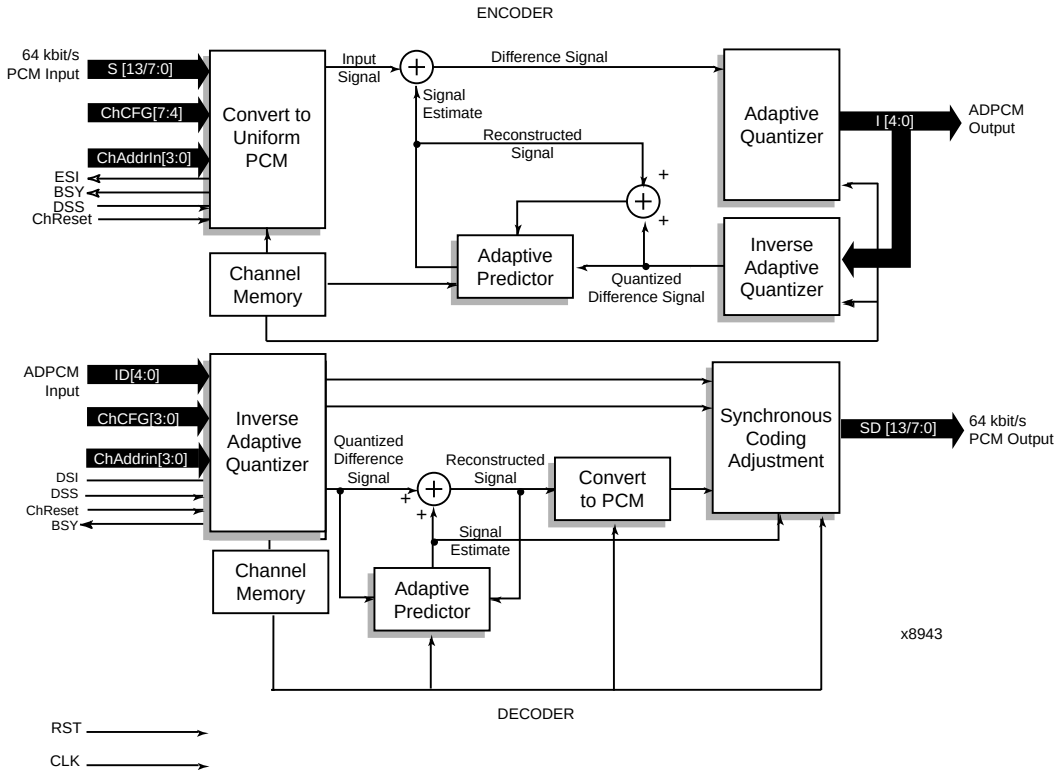

Figure 1: ADPCM Block Diagram

General Description

The ITU standard, G.726 includes the specifications of standards, G.721, G.723, G.726a, G.727, and G.727a. It specifies the requirements for the conversion of a 64 kbit/s pulse code modulation (PCM) channel to and from a 40, 32, 24 and 16 kbit/s channel, using an Adaptive Differential Pulse Code Modulation (ADPCM) transcoding technique.

The ISS ADPCM core is compliant with the G.726 standard and supports 8 duplex channel coding. The PCM input channel multiplexing and serial to parallel conversion circuitry may be added to suit the target system as required. The core is online configurable in terms of compression rates. It has been tested and verified to be fully compliant using the ITU standard test vectors.

Functional Description

The ADPCM is partitioned into modules as shown in Figure 1 and described below.

Encoder Operation

The ADPCM encoder consists of five functional blocks, namely Convert to Uniform PCM block, Channel Memory block, Adaptive Quantizer block, Inverse Adaptive Quantizer block, and Adaptive Predictor block. Subsequent to the conversion of the A-law or μ-Law PCM input signal to uniform PCM, a difference signal is obtained, by subtraction of an estimate of the input signal from the input signal itself. The adaptive 31-, 15-, 7-, or 4-level quantizer is used to assign five, four, three or two binary bits, respectively, to the value of the difference signal for transmission. The inverse quantizer produces a quantized difference signal from these same five, four, three or two binary bits, respectively. The signal estimate is added to this quantized difference signal to produce the reconstructed version of the input signal. Both reconstructed signal and quantized difference signal are operated upon by an Adaptive Predictor, which produces the estimate of the input signal, thereby completing the feedback loop. CLK, DSS, and ChReset signals control the encoder's operation for each duplex channel.

When ChReset signal is asserted, the control word, ChCFG, will be loaded to a corresponding Channel Memory, which is specified by the channel address, ChAddrIn. Meanwhile, a busy signal, BSY is set to high to indicate that

the encoder is in operation. When the encoder procedure is completed, the BSY is returned to low. During the encoding process, a signal, ESI, is used to indicate when a valid result is output.

Convert to Uniform PCM

When DSS is asserted, the Convert to Uniform PCM block reads data from the PCM input, and loads the control word from the Channel Memory to convert the data to a uniform PCM signal.

Channel Memory

This is 280 bits wide x N bits deep (N = 8, number of channels in this implementation) memory that stores the control word, ChCFG, is specified by the channel address, ChAddrIn. Channel Memory is embedded within the core and uses distributed memory in the FPGA.

Adaptive Quantizer

The Adaptive Quantizer block provides a specified compression rate, e.g. 16, 24, 32 and 40, specified by the channel control word, ChCFG, to quantize a difference signal for transmission.

Inverse Adaptive Quantizer

The Inverse Adaptive Quantizer block produces a quantized version of the difference signal by a scaling factor specified by the ChCFG.

Adpative Predictor

The primary function of the Adaptive Predictor block is to compute the signal estimate from the quantized difference signal. Two adaptive predictor structures are used, a sixth order section that model zeros and a second order section that models poles in the input signal.

Decoder Operation

The decoder includes a structure similar to the Inverse Adaptive Quantizer block and Adaptive Predictor block of the encoder, together with a uniform PCM to A-law or μ-law conversion and a synchronous adjustment.

Convert to PCM

This block is the counterpart of Convert to Uniform PCM block in the encoder. It performs uniform PCM to A-law or μ-law conversion.

Synchronous Coding Adjustment

The Synchronous Coding Adjustment block prevents cumulative distortion occurring on synchronous tandem coding (ADPCM-PCM-ADPCM, etc., digital connections) under certain conditions. The synchronous coding adjustment is achieved by adjusting the PCM output codes in a manner that attempts to eliminate quantizing distortion in the next ADPCM encoding stage. As in the encoder, the CLK, DSS and ChReset signals control the decoder's operation for each duplex channel.

Core Modifications

The ISS ADPCM core can be modified to meet specific design needs. Modifications include:

- Number of channels
- Compression ratios supported
- Coding laws supported (A-law or m-law)

Pinout

Pinout of the ADPCM core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are described in Table 1.

Verification Methods

Complete functional and timing simulation has been performed using Synopsys VSS and Model Technology ModelSim.

Recommended Design Experience

Users should be familiar with HDL design methodology and Xilinx design flows including VHDL/Verilog language and syntax, component instantiation, synthesis, and simulation.

Ordering Information

For information on the ADPCM core, please contact Integrated Silicon Systems directly from the address available on the first page of this datasheet.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Input Interface Signals		
S[13/7:0]	Input	Input word for encoding. Uniform PCM input uses all 14 bits, S[13:0] (A-law) or 13 bits, S[12:0] (µ- law). PCM input uses 8 bits, S[7:0]
ID[4:0]	Input	ADPCM input word ID[4] : bit no.1 the polarity ID[4:3] : 2-bit ADPCM word ID[4:2] : 3-bit ADPCM word ID[4:1] : 4-bit ADPCM word ID[4:0] : 5-bit ADPCM word
ChCFG[7:0]	Input	Configuration word ChCFG[7]:Encoding Law: 1 = A-law, 0 = µ-law ChCFG[6]:Encoding Even Bit Inversion: 1= Yes, 0 = No. ChCFG[5:4]:Encoding compress rates:00=16, 01=24, 10=32 and 11=40 ChCFG[3]:Decoding Law: 1 = A-law, 0 = µ-law ChCFG[2]:Decoding Even Bit Inversion:1= Yes, 0 = No. ChCFG[1:0]:Decoding compress rates:00=16, 01=24, 10=32 and 11=40
DSS	Input	Data strobe signal, active high
ChAddrIn[3:0]	Input	Channel address associated with input data
ChReset	Input	Individual channel reset input associated with ChAddrIn
RST	Input	Global reset input
CLK	Input	Clock input-rising edge active
I[4:0]	Output	ADPCM output word. I[4]: bit no.1 the polarity I[4:3]: 2-bit ADPCM output I[4:2]: 3-bit ADPCM output I[4:1]: 4-bit ADPCM output I[4:0]: 5-bit ADPCM output
SD[13/7:0]	Output	PCM output word. Uniform PCM uses all 14 bits, SD[13:0] (A-law) or 13 bits, SD[12:0] (µ-law). PCM uses 8 bits, SD[7:0]

Table 1: Core Signal Pinout (Continued)

Signal	Signal Direction	Description
BSY	Output	Codec operation indicator. 1 = operation 0 = free
ESI	Output	Encoding status indicator
DSI	Output	Decoding status indicator

Related Information

European Telecommunications Standards Institute

For information on European digital broadcasting systems standards contact:

European Telecommunications Standards Institute
6921 Sophia Antipolis Cedex
France
Phone: +33 92 94 42 00
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Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95214
Phone: 408-559-7778
Fax: 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: 800-231-3386 (inside the US)
408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE specific information, contact:

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Phone: 408-879-5381
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URL: www.xilinx.com/products/logicore/alliance/tblpart.htm