1024-Channel ADPCM

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Features

- Supports Virtex™-II devices
- Supports, G.721, G.723, G.726, G.726a, G.727, and G.727a ITU standards
- 1024 channel simplex/512 duplex encoding and decoding
- Online configurable for different compression rates, µ-law and A-law for each encoding or decoding channel
- Coding (encode or decode) for one data sample in 6 clock cycles (min)
- Can work in both burst and continuous modes
- Conforms fully to ITU test vectors

Applications

- Digital Enhanced Cordless Telecommunications (DECT)
- Video conferencing
- Telecommunications
- Voicemail systems
- Satellite communications
- VoIP

AllianceCORE™ Facts

Core Specifics	
Supported Family	Virtex-II
Device Tested	2V500-5
CLB Slices	2734
Clock IOBs[1]	1
IOBs[1]	68
Performance (Minimum Functional Clock)	50 MHz
Xilinx Tools	v3.2i
Special Features	18 Block RAMs
Provided with Core	
Documentation	User Guide, Design Guide
Design File Formats	EDIF netlist, VHDL RTL available extra
Constraints File	ADPCM1024.ncf
Verification	Testbench, Test Vectors
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	None
Additional Items	None
Simulation Tool Used	
ModelSim v5.3c	
Support	
Support provided by Amphion Semiconductor	

1. Assuming all core I/Os are routed off-chip.

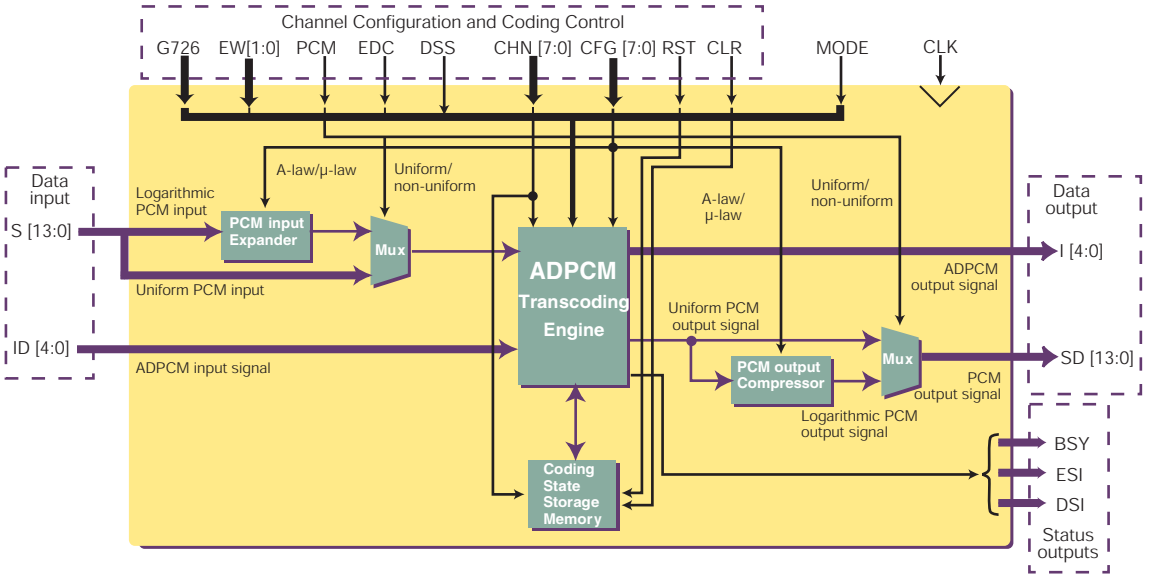

Figure 1: 1024 Channel ADPCM Block Diagram

General Description

The Amphion family of adaptive differential pulse code modulators (ADPCMs) is designed to provide high performance solutions for a broad range of applications requiring speech compression and decompression. These application specific virtual components (ASVCs) support up to 1024 simplex channels on Xilinx FPGA. Each channel is independently selectable for encoding or decoding, and are fully compliant with ITU G.726, G.726a, G.727 and G.727a standards.

The core supports 1024 simplex channels. The core is on-line configurable in terms of compression rates. It has been tested and verified to be fully compliant using the ITU standard test vectors.

Functional Description

The Amphion ADPCM core consists of 5 primary sections: a PCM Input Expander, an ADPCM Transcoding Engine, a PCM Output Compressor, a Coding State Storage Memory, and a Channel Configuration and Coding Control, as illustrated in Figure 1. The core operates on one input sample at a time, using 6 clock cycles to complete the encoding or decoding. Multichannel coding is implemented on time-multiplexing basis. The input/output channel multiplexing and serial to/from parallel conversion circuitry may be added to suit the target system as required.

The core has two channel addressing modes: the flexible mode and the duplex mode. In the duplex mode, half of the channels are set to encode and half to decode. The flexible mode allows each channel to be set, and reset, individually. Within each of these modes the core can encode data from three types of PCM format, as specified by ITU standard G.711, to 2, 3, 4 or 5-bit ADPCM format. These are 8-bit µ-law or A-law logarithmic PCM, 14-bit µ-law uniform PCM or 13-bit A-law uniform PCM. The core can also decode data from the 2, 3, 4 or 5-bit ADPCM format to the three types of PCM format.

The cores are on-line configurable in terms of compression rate and PCM law and allow on-the-fly selection of PCM/uniform PCM input/output. Each member of Amphion's ADPCM family has been tested and verified to be fully compliant using the ITU standard test vectors.

PCM Input Expander (Logarithmic PCM to Uniform PCM)

This block converts the input PCM signal from 8-bit A or µ-law logarithmic PCM format to a 13-bit A-law or 14-bit µ-law uniform PCM signal. This decoding is performed according to the G.711 standard.

ADPCM Transcoding Engine

The primary encoding and decoding operations of the Amphion ASVC take place within the ADPCM transcoding engine.

When encoding, the difference between the uniform PCM input signal with a prediction of this signal is calculated. The difference signal is then passed to an adaptive quantizer where 5, 4, 3 or 2 binary digits are assigned as its value, following the quantization methods stipulated by the G.726 or G.727 standards. The result is the ADPCM signal for transmission.

The current ADPCM signal is then used to predict the next signal estimate. It is fed to an inverse adaptive quantizer and the output is added to the current input signal estimate to determine the reconstructed version of the input signal. This signal and the output of the adaptive quantizer are then used by the adaptive predictor to determine the estimate of the next input signal, which is then fed back to determine the next difference signal.

When decoding, the reverse procedure is performed. First, the ADPCM signal is inversely quantized; then the resulting signal is added to a prediction of this signal, forming a reconstructed signal. The inversely quantized signal and the reconstructed signal are used by the adaptive predictor to determine the signal estimate for the next iteration.

This reconstructed signal is converted to a PCM signal before passing through an additional block needed for synchronous coding adjustment. This block prevents cumulative distortion occurring on synchronous tandem codings. This is when the signal is converted from PCM to ADPCM to PCM and back to ADPCM. The idea is that when the PCM signal is converted the resulting ADPCM signal is the same at every stage. The output PCM signal from this block is the resulting decoded output of the codec.

PCM Output Compressor (Uniform PCM to Logarithmic PCM)

This block converts the output PCM signal from either 13-bit A-law or 14-bit μ-law uniform PCM format to an 8-bit A- or μ-law logarithmic PCM signal. This encoding is performed according to the G.711 standard.

Coding State Storage Memory

The 1024 channel ADPCM algorithm requires 282 bit states for each encoding or decoding channel (i.e., 564 bits per duplex channel). These states are stored in the memory of the ADPCM core.

The total memory required by the core is N x 282 where N is the number of simplex channels available.

Channel Configuration and Coding Control

The 8-bit wide CFG bus determines the compression rate and law for each channel. The function of each bit is listed in Table 1. Note that the top 4 bits are only used in the duplex mode and specify the law and compression rate for encoding.

The input signal G726 is used to specify whether the G.726 or G.727 is in use; when high the core operates per the G.726 standard, low indicates G.727.

Duplex (that is, the channels are split evenly between encode and decode) and flexible channel addressing modes are selected via the static MODE input. When MODE is high, the core operates in duplex mode and when MODE is low the core operates in the flexible mode. In the latter case, each channel can operate as either an encoding or a decoding channel.

Table 1: Codec Configuration Control Word

CFG Bits	Description	Control Choice			
	Control Values	**0**		**1**	
[7]	Selects either A-law or μ-law for encoding in the duplex mode	μ-law		A-law	
[6]	Control whether even bit inversion is performed for A-law/μ-law encoding operations in duplex mode	No bit inversion		Even bit inversion performed for A-law. All bit inversion performed for μ-law	
	Control Values	**00**	**01**	**10**	**11**
[5:4]	Controls the number of bits in the ADPCM output word when encoding in duplex mode	2 bits	3 bits	4 bits	5 bits
Bits	**Control Values**	**0**		**1**	
[3]	Selects either A-law or μ-law for decoding in the duplex mode or encoding/decoding in the flexible mode	μ-law		A-law	
[2]	Controls whether even bit inversion/all bit inversion is performed for A-law/μ-law decoding operations in the duplex mode or encoding/decoding in the flexible mode	No bit inversion		Even bit inversion performed for A-law. All bit inversion performed for μ-law	
	Control Values	**00**	**01**	**10**	**11**
[1:0]	Controls the number of bits in the ADPCM output word when encoding in the duplex mode or the number of bits in the ADPCM input word and the ADPCM output word in the flexible mode.	2 bits	3 bits	4 bits	5 bits

It should be noted that:

- The core should be configured before an encoding or decoding operation is started.
- When core busy indicator BSY is HIGH, asserting the control signal DSS is ignored.
- Other input control signals, namely, EDC, CHN, PCM, G726 and EW, are latched on the clock rising edge when DSS is HIGH and BSY is LOW.
- Input data S and ID are also latched on the clock rising edge when DSS is HIGH and BSY is LOW.
- The output data is registered.
- The encoding status indicator ESI indicates the internal encoding state of the core. When it goes to LOW, the core has completed the predictor state update. When it returns to HIGH, the encoding output is available.
- The decoding status indicator (DSI) indicates the internal decoding state of the core. When it goes to LOW, the core has completed the predictor state update. When it returns to HIGH, the decoding output is available.
- When an encoding or decoding operation is completed, signal BSY returns to LOW and the core waits for DSS to be asserted to start the next operation.
- Encoding and decoding can be performed in any order.

Output signals encode status indicator (ESI) and decode status indicator (DSI) indicate the encoding and decoding status, respectively. From the cycle when the codec picks up the input data, ESI or DSI goes to ‘0’. In the cycle when the encoding/decoding output is available, the corresponding signal returns to ‘1’. Both the signals are set to ‘1’ after reset and before the first input.

Encoding/Decoding Operation

Encoding or decoding of one data sample is started by asserting the data strobe signal (DSS). The input select signal EDC defines whether the core performs an encoding or a decoding operation. When EDC is HIGH, the core performs encoding and the input S is taken. When EDC is LOW the core will decode and the input ID is taken. Input signal PCM specifies the type of encoding input data and decoding output data, and input CHN specifies the channel the data belongs to, as described in the previous sections.

The ADPCM core requires 6 clock cycles to complete an encoding or decoding operation for one data sample and the output indicator BSY is de-asserted after the rising edge of the 6th cycle. DSS can then be asserted after the rising edge to start the next operation.

Channel Selection

The CHN input specifies the channel with which the input data is associated when the core is performing a coding operation or with which the CFG word is applied when the core is performing channel reset and configuration. In the flexible mode, one channel is either encoding or decoding and the channel number is fully specified by CHN.

Global Reset and Configuration

The asynchronous global reset signal, RST, resets all the channels and configures them with the same compression rate and PCM law; reset is activated when RST is asserted. RST also resets all the registers in the core and interrupts the encoding/decoding operation the core is performing. Global configuration of the core is performed using the CFG input as described earlier. The reset and configuration process starts on the first rising clock edge after RST has been de-asserted and continues for N cycles, where N is the number of simplex channels (where each duplex channel is considered as two simplex channels).

Core Modifications

The Amphion ADPCM core can be modified to meet specific design needs. Modifications include:

- Number of channels
- Compression ratios supported
- Coding laws supported (A-law or μ-law)

Pinout

Pinout of the ADPCM core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Table 2 gives the descriptions of the input and output ports (shown graphically in Figure 2) of the 1024 ADPCM codec. Unless otherwise stated, all signals are active high and bit (0) is the least significant bit.

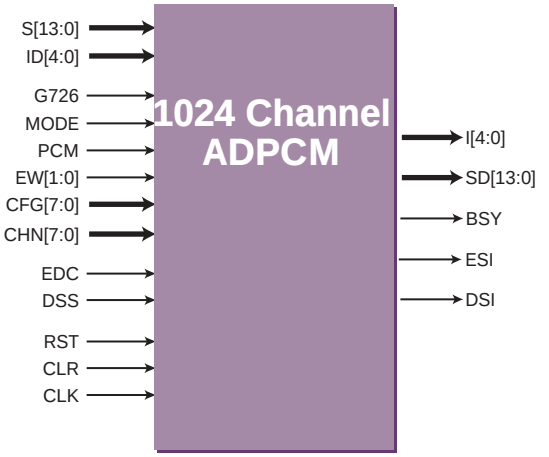

Figure 2: 1024 Channel ADPCM Core Pinouts

Table 2: Pinout Table

Signal	Signal Direction	Description
CLK	Input	Clock input. Rising edge active
RST	Input	Global reset input
CLR	Input	Synchronous individual channel reset and configuration signal, active high
MODE	Input	Selects between the two modes of operation for the ADPCM core, the duplex and flexible modes High: duplex mode Low: flexible mode
DSS	Input	Input data strobe signal, active high, encoding/decoding is started when asserted and BSY is low
EDC	Input	Selects encode or decode operation: High: encode Low: decode
PCM	Input	Logarithmic PCM or uniform PCM selection control signal High: logarithmic PCM Low: uniform PCM
S[13:0]	Input	Logarithmic or uniform PCM input word for encoding S[13:0]: µ-law uniform PCM input S[13:1]: A-law uniform PCM input S[7:0]: Logarithmic PCM input
ID[4:0]	Input	ADPCM input word for decoding ID[4:3] = 2 bit ADPCM word, 16 Kbits/sec data rate ID[4:2] = 3 bit ADPCM word, 24 Kbits/sec data rate ID[4:1] = 4 bit ADPCM word, 32 Kbits/sec data rate ID[4:0] = 5 bit ADPCM word, 40 Kbits/sec data rate
G726	Input	Specifies G.726 or G.727 operation High: G.726 standard Low: G.727 standard
EW[1:0]	Input	Specifies the number of G.727 enhancement bits "00" = 0 bits "01" = 1 bit "10" = 2 bits "11" = 3 bits
CHN[9:0]	Input	Specifies channel with which the input data is associated when the core is performing coding operation or performing channel reset. Duplex mode: one channel encoding/decoding (the LSB is ignored by the core). In the flexible mode, one channel coding is either encoding or decoding and the channel number is fully specified by CHN.
CFG[7:0]	Input	Channel configuration word - see Table 1 for details.
I[4:0]	Output	ADPCM output word I[4:3] = 2 bit ADPCM output, 16 Kbit/s I[4:2] = 3 bit ADPCM output, 24 Kbit/s I[4:1] = 4 bit ADPCM output, 32 Kbit/s I[4:0] = 5 bit ADPCM output, 40 Kbit/s
SD[13:0]	Output	Logarithmic or uniform PCM output word from decoding SD[13:0] = µ-law uniform PCM output SD[13:1] = A-law uniform PCM output SD[7:0] = Logarithmic PCM output
BSY	Output	Core busy indicator, active high, DSS is ignored when BSY is active
ESI	Output	Encoding status indicator
DSI	Output	Decoding status indicator

Verification Methods

Complete functional and timing simulation has been performed using Model Technology ModelSim.

Recommended Design Experience

Users should be familiar with HDL design methodology and Xilinx design flows including VHDL/Verilog language and syntax, component instantiation, synthesis, and simulation.

Ordering Information

For information on the 1024 channel ADPCM core, please contact Amphion directly from the address available on the first page of this datasheet.

Related Information

European Telecommunications Standards Institute

For information on European digital broadcasting systems standards contact:

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Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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