



YCrCb2RGB Color Space Converter

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Product Specification



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Features

- Converts digital component video (YCrCb) to digital RGB
- · Optimized for specific Xilinx architectures
- High-speed operation for HDTV applications
- · One conversion per clock cycle--throughput
- · Low latency: 6 clock cycles
- · All outputs properly limited
 - No external logic needed to handle these conditions
- VHDL source code and testbench included with core

AllianceCORE™ Facts				
Core Specifics				
See Table 1				
Pro	vided with Core			
Documentation	Core Design Document			
Design File Formats	VHDL source code, EDIF netlist			
Constraints File	yrb2rgb.ucf			
Verification	Testbench, test vectors			
Instantiation	VHDL, Verilog			
Templates				
Reference designs &	None			
application notes				
Additional Items	None			
Simulation Tool Used				
Active-HDL 3.5 (Aldec)				
Modelsim 5.e (Model Technology)				
Support				
Support provided by Perigee, LLC.				

Applications

Real-time component video to RGB graphics conversion

Table 1: Core Implementation Data

Supported Family	Device Tested	CLBs	Clock IOBs	IOBs ¹	Performance (MHz)	Xilinx Tools	Special Features
Virtex-E	V100E-8	188 ²	1	64	230	M2.1i	None
Virtex	V50-6	188 ²	1	64	154	M2.1i	None
4000E/EX/XL/XLA	4036XL-08	161	1	64	132	M2.1i	None
Spartan/XL	S20-4	161	1	64	97	M2.1i	None

Notes:

- 1. Assuming all core I/Os are routed off-chip.
- 2. Utilization numbers for Virtex and Virtex-E are in CLB slices.

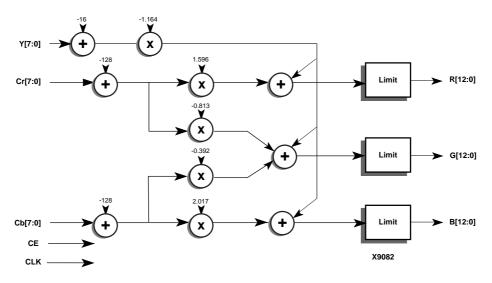


Figure 1: YCrCb2RGB Color Space Converter Block Diagram

General Description

Luminance and color difference coded signals (YCrCb) are generated by many component video systems. Conversion to RGB is necessary to feed a display device requiring RGB input. Figure 1 shows the converter block diagram.

Functional Description

The YCrCb to RGB color space converter is designed to perform the following equations:

The core has a latency of 6 clock cycles and a throughput of 1 clock cycle. Both input and output are registered for consistent routing and timing.

Multipliers

The multipliers are constant-coefficient and are optimized for Xilinx architecture.

Limiting

13-bit arithmetic is performed inside this logic core. The full precision of the results are brought out to the outputs of the core. However, there are cases where inputs can be provided such that the outputs will overflow. The limiting function protects against both positive and negative overflow conditions.

Core Modifications

Modified versions of this core or similar cores are available for purchase. Examples include:

- · Adjusting color channel bit widths
- · RGB2YCrCb color space correctors
- · Gamma-correctors

Contact Perigee directly for more information.

Pinout

The pinout of the color space converter has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in Figure 1 and described in Table 1.

Verification Methods

The core has been tested with in-house developed VHDL testbench and test vectors that are provided with the core.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
Y[7:0]	Input	Luminance
Cr[7:0]	Input	Color Red
Cb[7:0]	Input	Color Blue
CE	Input	Clock Enable
CLK	Input	Clock: uses one FPGA CLKIOB pin
R[12:0]	Output	Red
G[12:0]	Output	Green
B[12:0]	Output	Blue

Recommended Design Experience

Users should be familiar with video systems and Xilinx development tools.

Ordering Information

The product, as described, is available directly from Perigee, LLC.

Perigee also offers services and contract engineering for varying levels of development from logic design to system level embedded and bus-based products. These services include:

- · IC design, VHDL or schematic based
- Turnkey hardware/software/firmware development
- · System design
- · Board design
- · DSP and image processing
- · Embedded firmware
- · GUI and Application software

Perigee's particular area of expertise is in digital video and digital signal processing applications. For more information on Perigee, their products and services, contact them directly.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc. 2100 Logic Drive San Jose, CA 95124 Phone: +1 408-559

Phone: +1 408-559-7778 Fax: +1 408-559-7114 URL: www.xilinx.com

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tblpart.htm