1's and 2's Complement

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Features

- Supports 3 to 32 bit data
- Clock Enable for internal registers
- Uses fast carry logic for high speed
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

In 1's complement mode this macro accepts an N-bit value and inverts the data on a bit-by-bit basis when the INV signal is asserted (HIGH). In 2's complement mode this macro accepts an N-bit value and calculates the corresponding 2's complement value when the INV signal is asserted (HIGH). The data is passed through unchanged when INV is not asserted. The result is then registered.

The Truth Table for this function is shown in Table 1.

Table 1: Truth Table

INV	CE	C	Q
X	0	_/-	No Change
0	1	_/-	A
1	1	_/-	INV(A)

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 2.

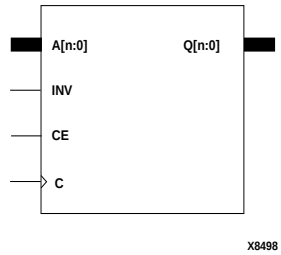

Figure 1: Core Schematic Symbol

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
A[n:0]	Input	A data input – value is inverted or 2's complemented when the INV signal is asserted.
INV	Input	INVERT DATA SIGNAL – the incoming data on A is bitwise inverted or 2's complemented when this signal is asserted.
CE	Input	CLOCK ENABLE – active high signal used to enable the transfer of data into the internal register.
C	Input	CLOCK – with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
Q[n:0]	Output	DATA OUTPUT - The registered output of the module.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Port Width**: Select an input bit width from the pull-down menu. The valid range is 3-32. The output width will be the same as the input width.
- **Create RPM**: When checked, a columnar Relational Placed Macro is created. This parameter is enabled only when the 1's Complementer type is selected, and is always true when 2's complement type is selected.
- **Twos Complement**: Select 1's Complementer or 2's Complementer.

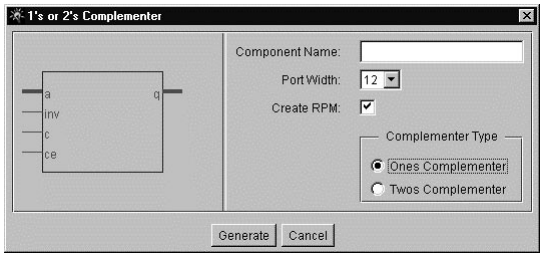

Figure 2: Parameterization Window

Core Resource Utilization

Table 2 shows the number of CLBs required for each available bit width.

Ordering information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Table 2: Bit Width versus CLB Count

Bit Width	CLB Count
2	1
3	2
4	2
5	3
6	3
7	4
8	4
9	5
10	5
11	6
12	6
13	7
14	7
15	8
16	8
17	9
18	9
19	10
20	10
21	11
22	11
23	12
24	12
25	13
26	13
27	14
28	14
29	15
30	15
31	16
32	16

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Port_Width	Integer	3 - 32
Create_RPM	Boolean	True/False
Twos_Complement	Boolean	True/False