LogiCORE

Synchronous FIFO
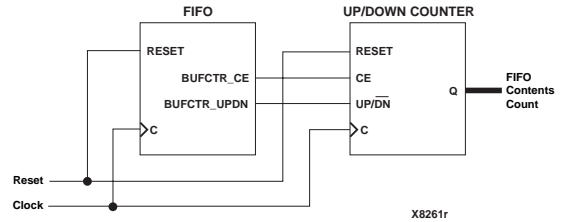
Product Specification

✕ XILINX®

Xilinx Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
E-mail: coregen@xilinx.com
URL: www.xilinx.com

Figure 1: Connections for Up/Down Counter

Features

• Supports data width from 4 to 80 bits
• Supports depths from 16 to 256 words
• Uses SelectRAM™ for high density and performance
• Registered output
• Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
• High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
• Available in Xilinx CORE Generator

Functional Description

The synchronous First-In, First-Out Memory module has a single clock port for both data-read and data-write operations. Data presented at the module's data-input port (D) is written into the next available empty memory location on a rising clock-edge when the write-enable input (WE) is High. The memory-full status output (FULL) indicates that no more empty locations remain in the module's internal memory, and that further data-writes must be avoided until the FULL output returns Low. Data can be read-out of the FIFO via the module's data-output port (Q) in the order in which it was written by asserting the read-enable input (RE) prior to a rising clock edge. The memory-empty status output (EMPTY) indicates that no more data resides in the module's internal memory, and that further data-reads should be avoided until the EMPTY output returns to LOW.
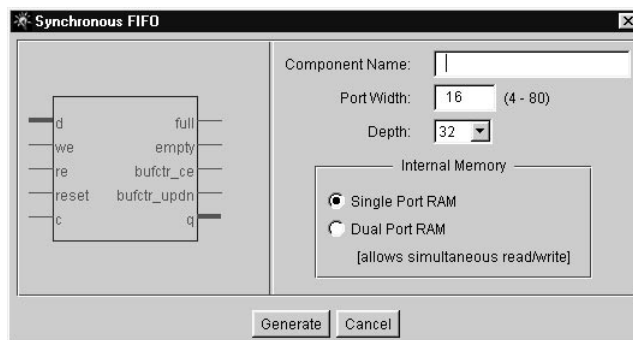
Figure 2: Parameterization Window
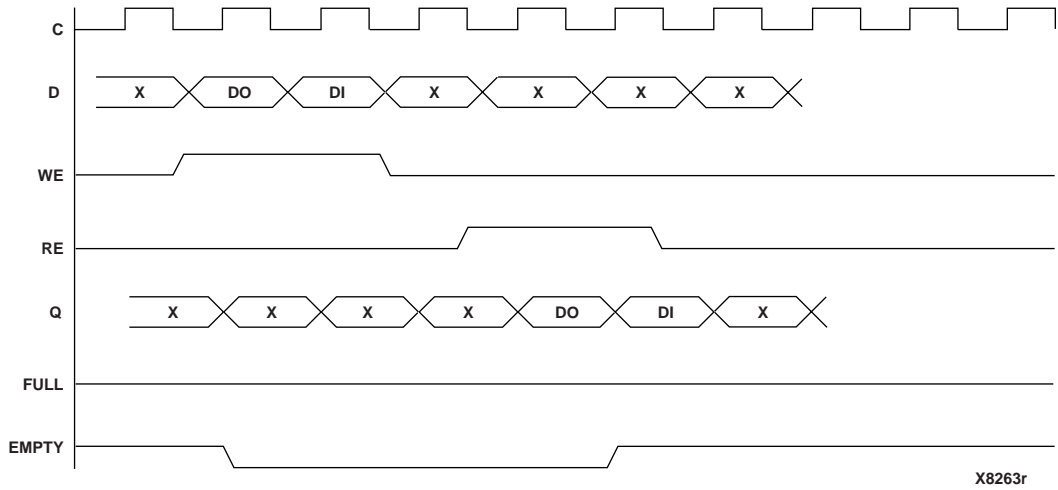
X8263r

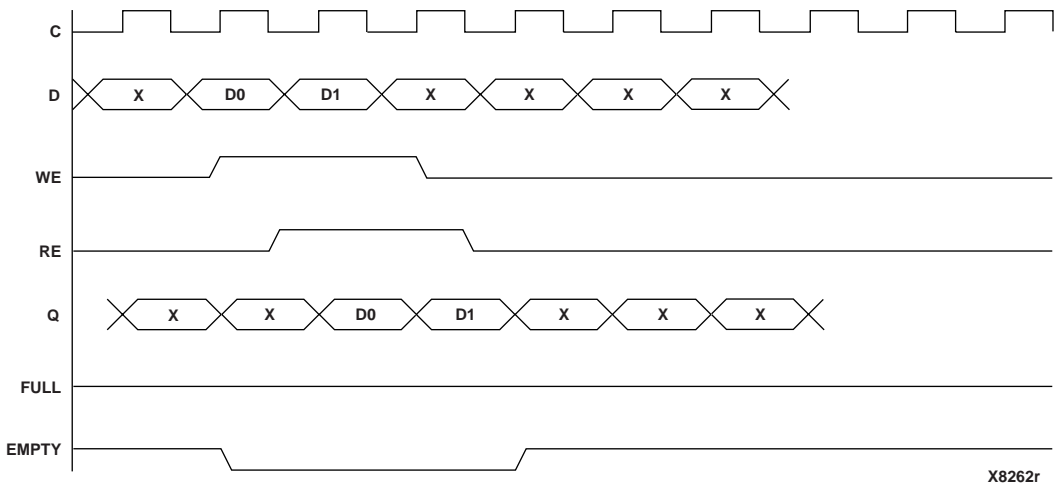**Figure 3: Timing Diagram for Single and Dual Ports**

X8262r

Figure 4: Timing Diagram for Dual Ports - Simultaneous Read and Write

Note: Data output Q contains valid data only during those cycles that were preceeded by an active read enable (RE). At all other times, the data output is in a don't care state and may actually assume the value of previously written data.

The internal read and write counters that maintain the FIFO status can be reset by asserting the RESET input prior to a rising clock edge. This effectively empties the FIFO, discarding any data that may have been stored in the module but which had not been read-out. Note that RESET has priority over RE and WE. The FIFO provides two additional outputs - BUFCTR_CE and BUFCTR_UPDN - that may be used to control an external up/down counter such that the counter's output indicates the number of data words that are currently stored in the FIFO. See Figure 1. This may be useful in applications where more information about the FIFO's empty/full status is required - such as half-full, for example.

The FIFO offers the designer the choice of implementing its internal memory with single- or dual-port SelectRAM™. Single-port memory is the most area efficient, but has the restriction that data may not be written and read at the same time. (I.e. WE = High and RE = High is illegal - and will be ignored - when single-port memory is used.) Dual-port memory permits simultaneous data-read and data-write operations, but incurs a higher area cost. See Figures 3 and 4.

The FIFO's internal state machine masks attempts to write data into a full FIFO (i.e. WE = High when FULL = High) and attempts to read data from an empty FIFO (i.e. RE = High when Empty = High). Either of these erroneous situations will be ignored by the FIFO, although no error flag is generated to indicate that the requested operation has not occurred.Pinout

Port names for the schematic symbol are shown in Figure 5 and described in Table 1. Timing diagrams for the single and dual port FIFOs are shown in Figures 3 and 4.
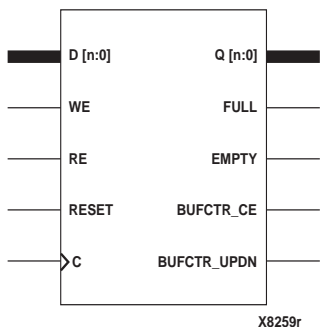
Table 1: Core Signal Pinout

Signal	Signal Direction	Description
D[n:0]	Input	DATA INPUT – port through which data is written into the FIFO.
WE	Input	WRITE ENABLE – active high signal used to allow the transfer of data from the input data port into the FIFO.
RE	Input	READ ENABLE – active high signal used to allow the transfer of data from the FIFO onto the output data pins.
RESET	Input	SYNCHRONOUS RESET – clears the FIFO
C	Input	CLOCK – with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
Q[n:0]	Output	REGISTERED DATA OUT – the registered output of the FIFO.
FULL	Output	FULL – this signal is asserted when the FIFO is full.
EMPTY	Output	EMPTY – this signal is asserted when the FIFO is empty.
BUFCTR_CE	Output	Optional connection to the clock enable of an external up-down counter.
BUFCTR_UPDN	Output	Optional connection to the up-down pin of an external up-down counter.

X8259r

Figure 5: Core Schematic Symbol

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Port Width**: Select an input bit width from the pull-down menu. The valid range is 4-80.
- **Depth**: Select the number of words in the FIFO from the pull-down menu. The valid range is 16-256 in multiples of 16.

- **Internal Memory**: You must choose Dual Port if simultaneous read/write operations are requiredCore Resource Utilization

Table 2 shows the resource utilization required for a sample of the available depths and bit widths.

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information, contact your local Xilinx sales representative or e-mail requests to coregen@xilinx.com.

Table 2: Synchronous FIFO Characterization Data

Depth	Data Width	Ports	CLB Count	Area Required for RPM[3] (Rows, Columns)	4000XL-08 (Advanced) MHz	4000XL-09 MHz	4000XL-3 MHz	Spartan-4 (Advanced) MHz
16	4	Dual	13	5,3		89	64	85
16	4	Single	13	4,4				
16	8	Dual	17	8,3		84	59	81
16	8	Single	15	4,4				
16	16	Dual	25	16,3		76	53	72
16	16	Single	19	8,4		80	55	78
16	32	Dual	41	32,3		62	44	
16	32	Single	27	16,4		68	49	68
16	48	Dual	57	48,3				
16	48	Single	35	24,4				
16	64	Dual	73	64,3				
16	64	Single	43	32,4				
16	80	Dual	89	80,3				
16	80	Single	51	40,4	66	59	41	
32	4	Dual	24	5,5		62	44	61
32	4	Single	18	5,4		80	58	69
32	8	Dual	36	8,5		59	41	58
32	8	Single	22	8,4		75	52	64
32	16	Dual	60	16,5		56	40	55
32	16	Single	30	16,4		67	48	58
32	32	Dual	108	32,5		50	35	
32	32	Single	46	32,4		58	40	
32	48	Dual	156	48,5				
32	48	Single	62	48,4				
32	64	Dual	204	64,5				
32	64	Single	78	64,4				
32	80	Dual	252	80,5				
32	80	Single	94	80,4				
64	4	Dual	32	6,6		58	39	54
64	4	Single	27	5,7		60	41	58
64	8	Dual	48	9,6		53	35	48

Depth	Data Width	Ports	CLB Count	Area Required for RPM[3] (Rows, Columns)	4000XL-08 (Advanced) MHz	4000XL-09 MHz	4000XL-3 MHz	Spartan-4 (Advanced) MHz
64	8	Single	35	5,7		58	39	56
64	16	Dual	80	17,6	52	46	32	43
64	16	Single	51	9,7		54	37	52
64	32	Dual	144	33,6		39	27	N/A
64	32	Single	83	17,7	57	51	35	44
64	48	Dual	208	49,6				
64	48	Single	115	25,7		48	32	
64	64	Dual	272	65,6				
64	64	Single	147	33,7		48	33	
64	80	Dual	336	81,6				
64	80	Single	179	41,7		41	28	
128	4	Dual	53	6,10		51	36	52
128	4	Single	41	6,11		59	41	53
128	8	Dual	85	9,10		48	34	42
128	8	Single	57	6,11		55	39	51
128	16	Dual	149	17,10	48	43	30	38
128	16	Single	89	9,11		53	37	49
128	32	Dual	277	33,10		36	25	
128	32	Single	153	17,11	56	50	35	42
128	48	Dual	405	49,10				
128	48	Single	217	25,11		49	34	
128	64	Dual	533	65,10				
128	64	Single	281	33,11		44	30	
128	80	Dual	661	81,10				
128	80	Single	345	41,11				
256	4	Dual	94	7,18	54	48	33	
256	4	Single	66	6,19	57	50	35	
256	8	Dual	158	9,18	51	45	31	
256	8	Single	98	6,19	54	48	34	
256	16	Dual	286	17,18	46	41	28	
256	16	Single	162	9,19	52	46	32	
256	32	Dual	542	33,18				
256	32	Single	290	17,19				
256	48	Dual	798	49,18				
256	48	Single	418	25,19				
256	64	Dual	1054	65,18				
256	64	Single	546	33,19				
256	80	Dual	1310	81,18				
256	80	Single	674	41,19				

Notes: 1. To achieve the performance documented in this table, it may be necessary to specify a TIMESPEC (timing specification) PERIOD constraint appropriate to meet the documented frequency.

2. For some parameter combinations, this core is not 100% relationally placed. Therefore the core's performance in your application may vary.

3. The RPM dimension shown provide guidance for selecting a device with the appropriate CLB array size.

Parameter File Information

Parameter	Type	Notes
Port_Width	Integer	4 - 80
Depth	Integer	16 - 256
Address_Width	Integer	4 - 8
Dual_Port	Boolean	True/False