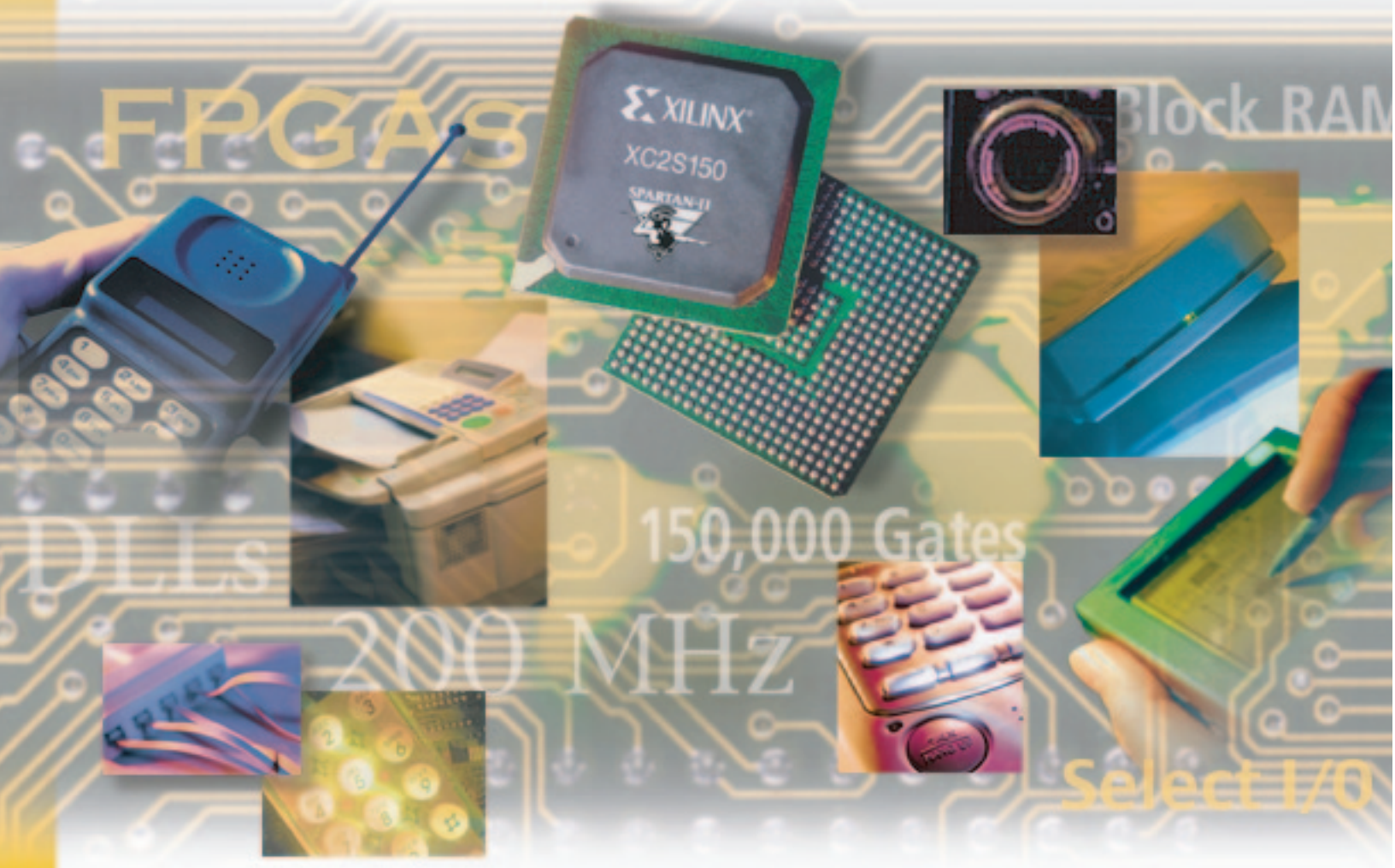
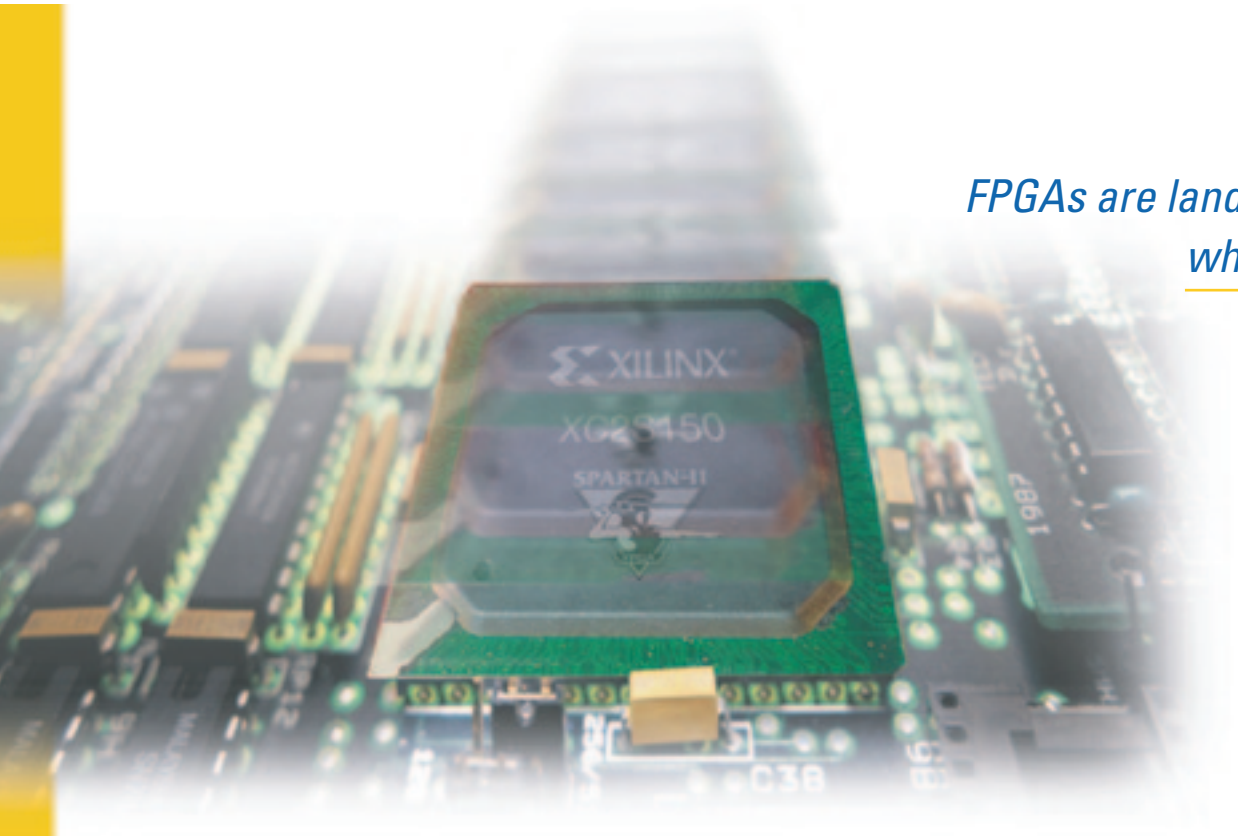
Make of it What You Will.

SPARTAN-II



XILINX®



FPGAs are landing where ASICs once did.

Where have all the ASICs gone?

The Spartan™ Series has been no friend to the ASIC. Since introduction in 1998, Spartan families have penetrated markets traditionally dominated by ASICs. Incredibly low price points have proved Spartan devices a viable solution, even when the products are extremely cost-sensitive.

Moving into ASSP territory.

It's happening with PCI controllers. With set-top boxes. Modems. Office equipment. Name your digital device. FPGAs are bumping ASSPs off the board and out of favor. But not so fast. Any old FPGA can't rightfully replace application specific parts. Only Spartan-II FPGAs can.

The Spartan-II family offers designers the complete package. Compare density, features and performance and the race runs neck and neck. But then factor in the enormous value of the programmability you get with FPGAs and the Spartan-II solution gains a big lead on its ASSP/ASIC counterparts. And before you issue any purchase orders, you better assess the costs. Get this: Spartan-II FPGAs give you 100,000 gates for under $10.

What do you make of all that? You make the leanest, meanest datacom, telecom, computing, and consumer products imaginable.

The flexibility of field upgrades.

The programmable capabilities of Spartan FPGAs give designers an edge that might just wipe ASICs and ASSPs right out of the picture in many markets. You can get your product to market faster because you're working with a standard part. When you order them, we ship them. But perhaps even more importantly, it means you can extend the time your product spends with its customers because Spartan devices can be upgraded in the field. Upgrading is as simple as downloading software. Imagine the possibilities.

A smaller die and a much bigger idea

With the new Spartan-II family, Xilinx went with the best process technology possible to produce a product with the smallest die size and the highest value to a system designer.

Get your free gates.

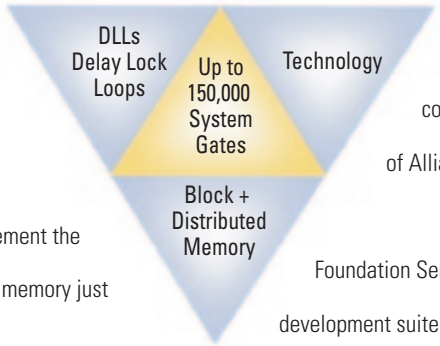
The Spartan-II family features five devices—with densities up to 150,000 gates—sold at some seriously aggressive prices. In fact, $10 gets you as many as 100,000 gates. With the Spartan-II feature set, many ASSPs become unnecessary. Spartan-II FPGAs can replace them without consuming any of the device's gates. The gates are essentially free.

Say goodbye to the gap.

Most designers will recall when it came to performance and features, there was a substantial gap between ASICs and FPGAs. Spartan-II FPGAs close the gap.

Memory to the max.

On-chip memory is a must and it's especially useful if it gives you a good deal of flexibility. Spartan-II FPGAs give you memory choices in the biggest way. Distributed memory and Block RAM efficiently implement the configuration that best suits you, or access external memory just as fast as the on-chip variety.



The clocks that rock.

If you have clock management woes, the Spartan-II family's four highly flexible DLLs will get you in sync. Integrated DLLs offer a wealth of new options. Designers can multiply or divide the incoming clock on a chip as well as drive multiple clocks on the board.

Purveyors of performance.

There are a lot of demanding new I/O standards in today's digital world. Spartan-II devices support them all with what we call Select I/O™ technology. You can lose the transceivers that devour dollars and real estate. Then you can hit the gas. I/O speed with these warriors blazes at over 200 MHz.

Powering down.

With portability in mind, Xilinx developed a nice power management plan. Each device has a power-down pin, which can put it to sleep. Core voltage is 2.5V, but interfacing with 3.3V and 5V circuits poses no problems.

How do you make complex design simple?

You take advantage of the many shortcuts Xilinx has put in place to help simplify your design tasks. Design with Spartan-II FPGAs and you'll have no costly NRE charges. And you'll have access to the industry's largest line up of highly complex cores, including 32 and 64-bit PCI plus a wide variety of AllianceCORE™ partner offerings.

Spartan-II devices are fully supported by the Xilinx Foundation Series™ software, which provides a complete development suite. All the EDA tools from Xilinx Alliance third-party partners are also supported to facilitate synthesis-based designs. Spartan-II designs get done in minutes so you spend less time waiting and more time working.

Summary

Spartan-II FPGAs offer an outstanding combination of density, performance, and features at prices competitive with ASICs in high volume. Coupled with lightning-fast design tools and a broad suite of intellectual property, the Spartan-II family is your complete high volume logic solution.

SPARTAN™-II

FPGA

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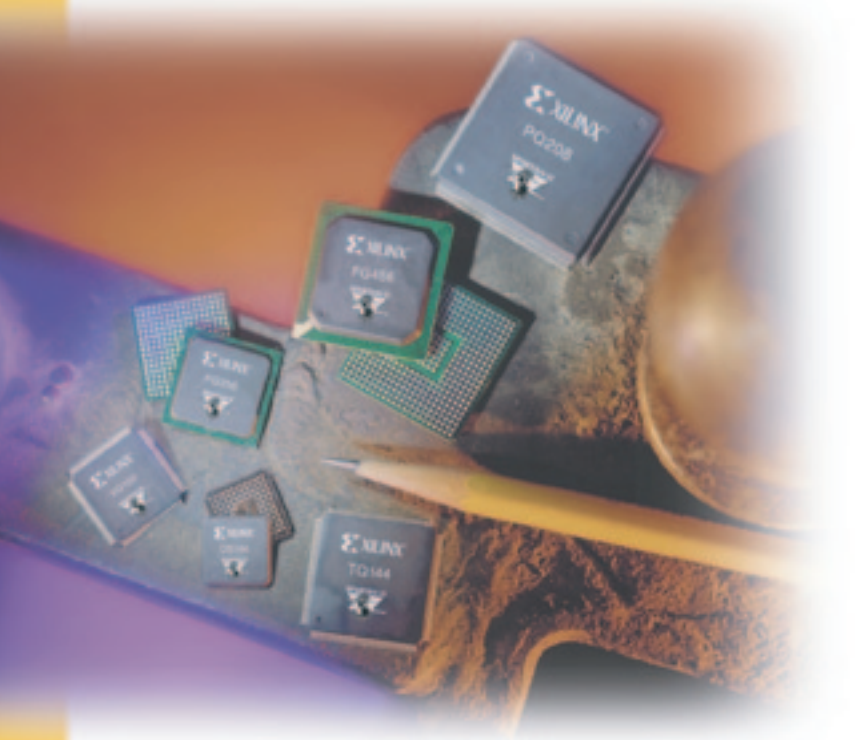

Robust Feature Set

- Flexible on-chip memory
  Distributed and Block Memory
- 4 Digital Delay Lock Loops per device
  Efficient chip level/ board level clock management
- Select I/O Technology
  Interface to all major bus standards
  HSTL, GTL, SSTL, etc…
- Full PCI compliance
- System speeds over 200 MHz
- Power Management (Sleep Mode)

Extensive Design Support

- Complete suite of design tools
- Extensive core support
- Compile designs in minutes

Advantages over ASICs

- No costly NRE charges
- No time consuming vector generation needed
- All devices 100% tested by Xilinx
- Field Upgradeable
- No lengthy prototype or production lead times
- Priced aggressively against comparable ASICs

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Spartan-II Product Matrix

Device		XC2S15	XC2S30	XC2S50	XC2S100	XC2S150
System Gates		15K	30K	50K	100K	150K
Logic Cells		432	972	1728	2700	3888
Block RAM Bits		16,384	24,576	32,768	40,960	49,152
Max I/O		86	132	176	196	260
Packages	14 x 14 mm	VQ100	VQ100			
	20 x 20 mm	TQ144	TQ144	TQ144	TQ144	
	12 x 12 mm	CS144	CS144			
	28 x 28 mm		PQ208	PQ208	PQ208	PQ208
	17 x 17 mm			FG256	FG256	FG256
	23 x 23 mm				FG456	FG456

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