The Spartan-II Family – The Complete Package

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Introduction

The Spartan™-II Family, Combined with a Vast Soft IP Portfolio is the First Programmable Logic Solution to Effectively Penetrate the ASSP marketplace.

Spartan-II FPGAs offer more than 100,000 system gates at under $10 and are the most cost-effective PLD solution ever offered. They build on the capabilities of the very successful Virtex family and supports all the associated features, including SelectIO™, BlockRAM™, Distributed RAM, DLLs, and support clock speeds up to 200 MHz. Spartan-II extends the Spartan family focus in competing against ASICs and is uniquely poised to penetrate the ASSP marketplace.

The Evolving ASIC/ASSP Landscape

The ASIC marketplace is currently undergoing major change. Traditional ASIC vendors are rapidly positioning their ASICs to address specific application areas and are moving away from using a generic ASIC strategy, leading to a decrease in the number of ASIC design starts. The high NRE and engineering costs involved in the development of an ASIC have forced designers to adopt an ASIC only if the volumes or the revenue are large enough to justify the investment. The ASIC design starts are also significantly affected by the success of PLDs, which dominate the gate-array market and are now beginning to encroach on the ASIC/ASSP marketplace.

Definitions: (Sidebar)

- **ASIC**. Describes all IC products dedicated to a specific application that are customized for a single user.
- **ASSP**. Describes all IC products dedicated to a specific application market that are sold to more than one user.
- **PLD**/**FPGA**.PLDs are defined as ICs programmed after assembly. This term broadly covers CPLDs and FPGAs.

Bryan Lewis, a key analyst at Dataquest, notes the following key transitions in the ASIC industry:

> *"The ASIC industry is in a major state of flux as traditional suppliers remold existing business plans to battle emerging suppliers with all new business plans. Design services, IP, and foundries are altering the course for the traditional ASIC supplier. Top ASIC suppliers are reorganizing around vertical application markets and are offering high-end products with increased margins. Top Americas-based companies lead the wave of reorganizations around vertical markets, but the rest are soon to follow. Lucent Technologies, IBM, and LSI Logic have clearly demonstrated that a vertical-market orientation is mandatory to compete in the emerging complex world of system-level integration."*

Programmable logic devices have been very successful in taking over gate arrays and are now making meaningful forays into the ASIC space. The dynamics in the ASIC/ASSP marketplace is opening up new opportunities for PLDs and allows them to compete against ASSPs.

The Spartan-II family has all the unique ingredients and enables Xilinx to successfully penetrate the ASSP marketplace.

PLDs Penetrating the ASSP Market

In the past, programmable logic devices have had limited success in penetrating the ASSP market because PLDs have lacked the density, features, performance, and most importantly, the cost to enable successful penetration. Bringing programmability and its traditional benefits to a design solution is always an expensive proposition and PLDs have traditionally lost the battle to the cost-optimized custom solution or ASIC.

PLD Evolution and Competing against ASSPs

PLDs however have been successful in replacing discrete TTL chips and providing a cost-effective and higher performance solution. PLDs have also had limited success in absorbing small memory devices, PALs, and UARTs onto a single chip. Apart from these examples, PLDs have had sparse victories over the last decade or so. PLDs, in spite of all the inherent advantages, have faced severe opposition in their forays into the ASSP market place (Figure 1).

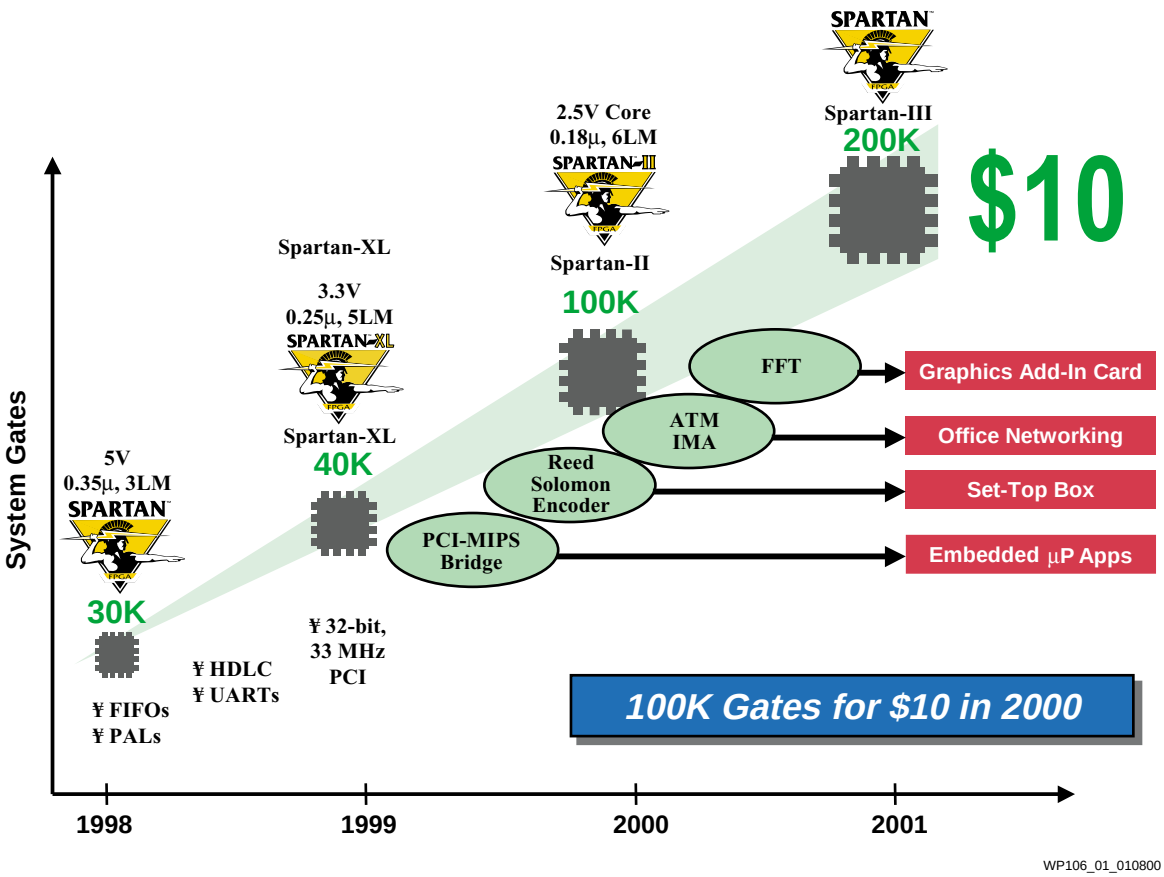

Figure 1: PLD Evolution—Addressing ASSP Marketplace

The playing field however has been leveled due to the use of cutting edge process technologies. This approach has allowed PLDs to significantly reduce die sizes, and therefore reduce the cost of the overall solution. This rapid transition in process technology has allowed PLD vendors to offer pad-limited programmable logic solutions. This in turn allows a PLD vendor to compete with an ASIC/ASSP on a per pin basis, and has opened up new markets for PLDs.

PLD vendors began to see the benefits of this approach in their biggest success story to date—the creation of a PCI Master/Target Controller. PLD vendors have been able to bring to the marketplace a 32-bit, 33 MHz, PCI Master/Target controller at half the price of an ASSP that offers the same functionality.

PLD vendors have actually been able to release a 64-bit, 66 MHz version of the PCI Master/ Target controller much earlier than most ASSP/ASIC vendors, and still maintain about half the price of an equivalent ASSP. The underlying programmable nature to the solution further bolsters the value of a **Programmable ASSP Solution**. An end customer can choose to use the PCI solution as sold by the PLD vendor or choose to augment or change the solution to best suit their needs. This is a testimonial to the tremendous potential that PLD vendors have for addressing the ASSP marketplace.

Understanding the Dynamics between ASSPs and PLDs

The biggest value that an ASSP offers a designer is that it allows faster time-to-market at a relatively low cost. However, ASSPs do not inherently allow for product customization and differentiation. For example, customers choosing stand-alone PCI devices from ASSP vendors almost always use a PLD to allow for product customization.

ASSP vendors are being pushed by market dynamics to accommodate flexibility and product customization. The competition in the ASSP marketplace is severe, and being late to service the demands of the end customer means lost opportunity and loss of market leadership. Development windows are also shrinking rapidly and this is especially true in emerging markets, where the ASSPs have traditionally charged a premium because they were available first. The result is that ASSP vendors must offer capabilities that have been the traditional strongholds of PLDs, such as flexibility, product-customization, and reduced development window. Network processors are prime examples of the ASSP vendors reacting to the market dynamics to accommodate product customization and development windows.

Aggressive Process technology adoption has also allowed PLDs to obtain more die per wafer, provide more logic, offer increased performance, and accommodate the various ASIC-like features required to allow system integration. This has been fundamentally instrumental in narrowing the wide gap between FPGAs and ASSPs. PLD vendors, by virtue of the benefits reaped through process technology now have the capability to service the needs of today's ASSP designers.

The Spartan-II family is extremely well positioned to offer a low-cost programmable ASSP alternative and expands the time-to-market advantage that PLDs traditionally offer (Figure 2). It also increases the value of the ASSP by allowing end users to customize their solutions.

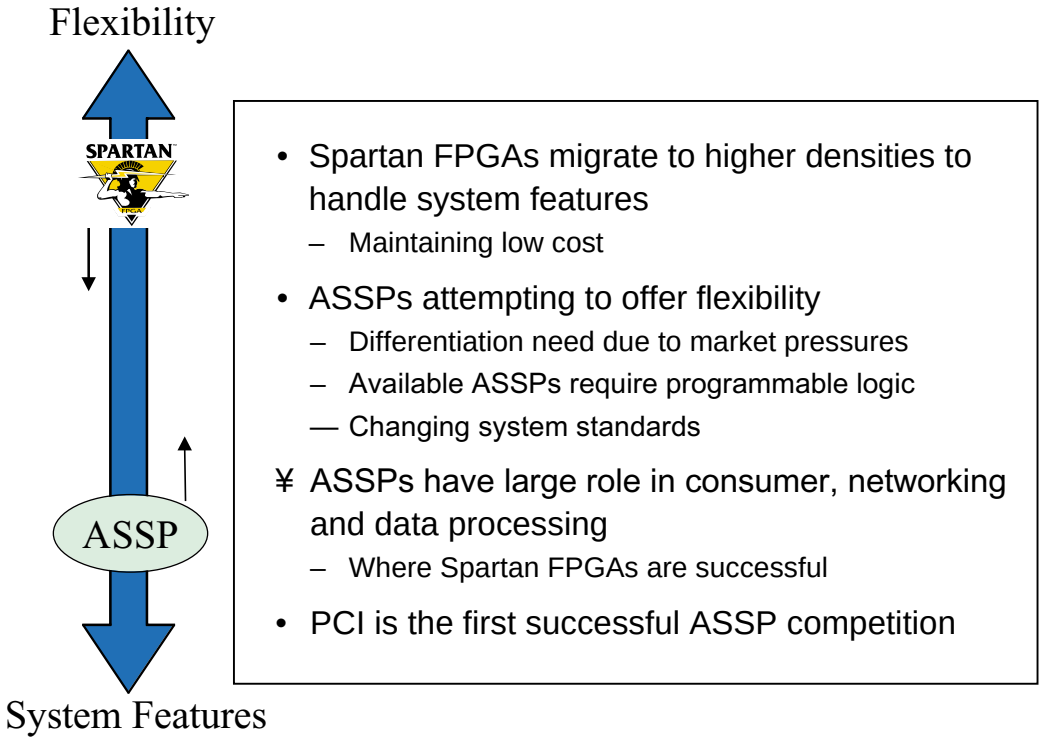

Figure 2: Spartan-II Penetrates ASSP Markets

Advantages of a Programmable ASSP

A programmable ASSP like the Spartan-II family offers significant advantages over a stand-alone ASSP. The advantages are broadly classified and discussed under the following areas:

- Value Proposition against ASSPs
- Accommodating Specification Changes
- Testing and Verification
- Xilinx On-line—Field Upgradability
- Issues in creating a stand-alone ASSP

Value Proposition against ASSPs

ASSPs designed for a wide array of designers are rarely able to meet every designer's exact needs. ASSPs need to be generic enough to be considered for wide applicability and use. This requires the designer to add their value proposition by using PLDs or ASICs around ASSPs to differentiate their product in the marketplace. This results in increased cost, increased board area, and reduced performance. There may also be instances where the designer does not need all the functionality built into a stand-alone ASSP. A stand-alone ASSP gets a designer closer to the eventual solution but rarely completes the circle.

With a programmable ASSP solution like Spartan-II, the designer can choose the right feature set and optimize their ASSP to achieve best possible results. Designers can also integrate their value proposition within the same piece of silicon and, to product customization and reduce costs.

The PCI case study shown in Figure 3 is a good example. A Spartan-XL PCI solution was able to effectively cut the total product cost in half and also allow room to accommodate the extra logic that a designer may want to add to the backend of their PCI interface such as a DMA controller, FIFO, or SDRAM controller.

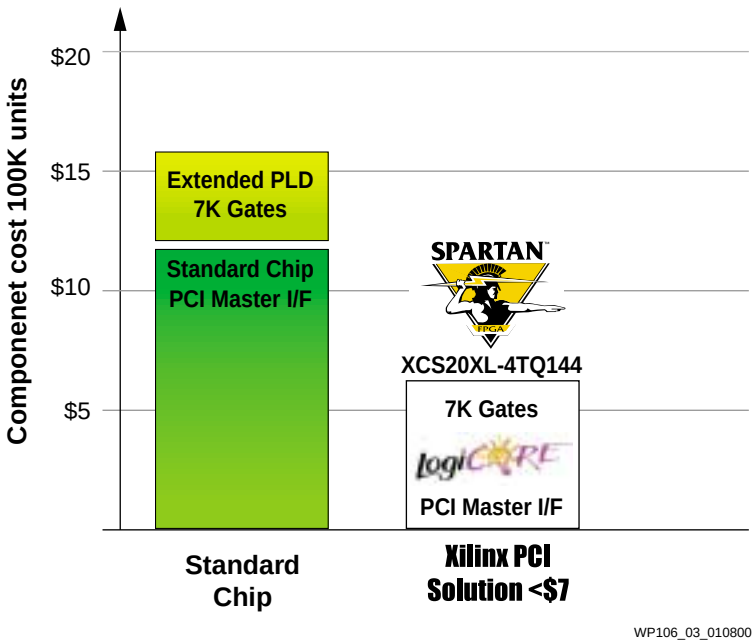

Figure 3: Xilinx PCI Solution Vs. Stand-alone ASSP

Accommodating Specification Changes

Stand-alone ASSP vendors are very motivated to create solutions for emerging markets because of the high profit margins they stand to gain. This is especially true in the datacom, telecom, and consumer markets. However, the standards change constantly in these markets and pose severe problems to the ASSP vendors.

As an example, the increased demand for bandwidth created by Internet users has created a huge marketplace for Digital Subscriber Line (DSL) solutions. The lack of a unified standard has been a key issue that has slowed the deployment of DSL services. The range of technologies that have been deployed reflects the difficulty of the problem being solved. There are at least six different technologies that have been adopted by various companies and it is still not clear who is going to emerge as the eventual winner.

Yet another example is Digital TV. The FCC established the DTV broadcast standard, which is actually a set of 18 different transmission standards that allow stations to use and switch between any of the 18 different formats that combine various combinations of screen ratios, numbers of horizontal and vertical lines of resolution, and two scanning methods. Among broadcasters, there is little resistance in moving to digital television, but there is some concern over which format to use. As noted in Figure 4, each U.S. network has selected or is leaning toward its preferred digital broadcast standard. It is very likely that a local station may support a different broadcast standard than its nationwide parent network.

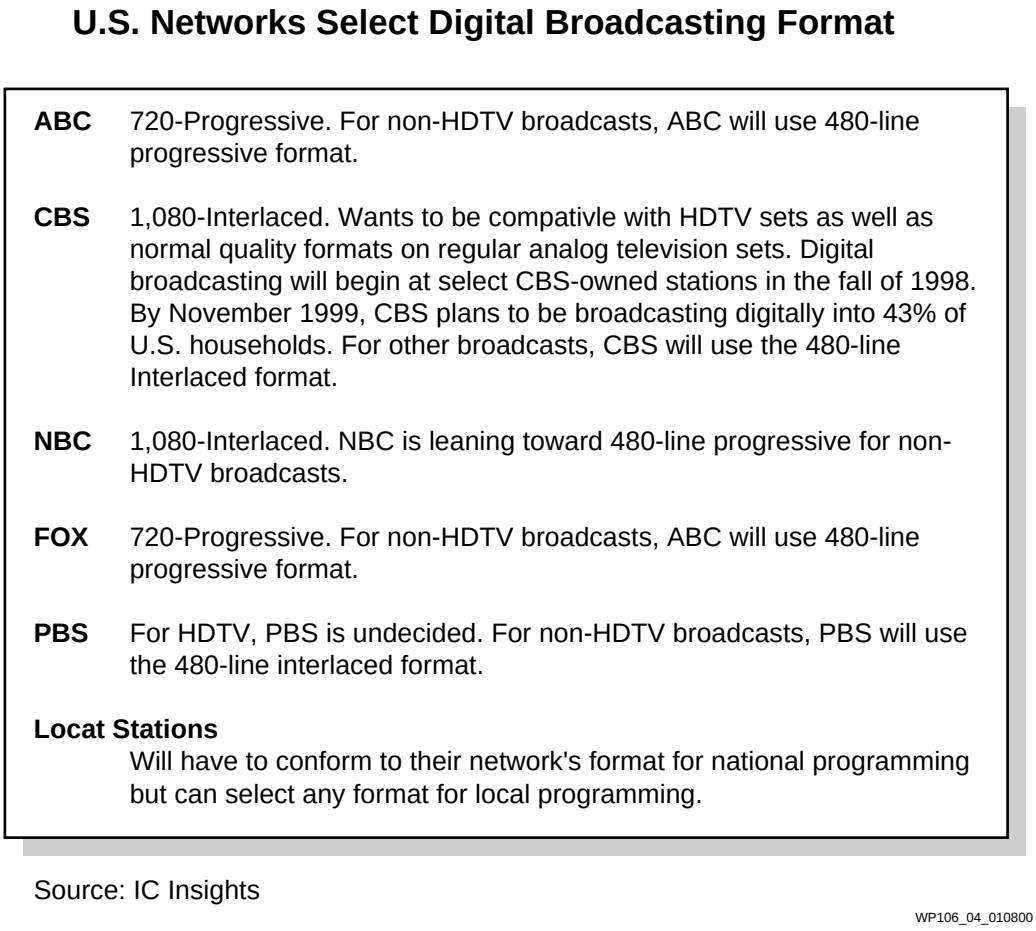

Figure 4: Different Digital Broadcast Standards Chosen by TV Networks

Conflicting specifications and lack of a clear direction create the need for programmable ASSP solutions. It is also quite likely that some of these conflicts may never get resolved. It would be nearly impossible and cost-prohibitive for an ASSP vendor to cater to all the various specifications. But, at the same time betting on the success of one single product may preclude them from being successful in the marketplace.

These conditions create many opportunities for the Spartan-II family—the industry's first programmable ASSP. Because of the high profit margins involved with these products, designers can easily continue using programmable ASSPs in volume production.

The Spartan-II family will not be able to compete against all ASSPs. But, it will hold it's own in many applications and specifically in new emerging datacom, telecom, and consumer markets.

Testing and Verification

Another problem users encounter with stand-alone ASSPs is that device do not always behave as expected. This can happen due to many different reasons, ranging from bugs in the silicon, system integration issues, software drivers, or even user error. Irrespective of the cause, verifying device problems can be very difficult with ASSPs. Verifying and identifying problems is a lot easier with programmable ASSPs. A programmable ASSP, such as the Spartan-II family, is built on the fabric of a proven FPGA technology and the silicon has been pre-verified and guaranteed to perform. This narrows the potential problems to a software-only issue and Xilinx provides powerful tools that improve the transparency of the final solution. Designers with the help of HDL simulators, test benches, and run-time debugging tools like ChipScope can easily identify the problem. Because a programmable ASSP is inherently re-programmable, fixing the problem is also simple. This is a tremendous value-add feature that a stand-alone ASSP cannot offer.

Xilinx On-line—Field Upgradability

Remotely updating software, with new enhancements and bug fixes, is fairly common in the electronics industry. Remotely updating hardware in this same manner might seem more challenging because the system hardware is typically a fixed entity that can only be updated by manual replacement (board swapping). However, creating hardware that can be upgraded in the field can significantly increase the useful lifetime of a system. The ability to add new hardware features and fix bugs without sending a technician out to the field can add up to considerable maintenance and support savings over the entire life of the system.

Designing systems that do remote upgrades can also provide new revenue opportunities. After the initial product is released, new hardware features can be developed, sold and distributed inexpensively to existing customers in much the same way as new versions of software can be distributed today. In addition, a standard "off-the-shelf" application can be developed so that features can be swapped in and out depending on what the end-user purchases or needs.

Xilinx FPGAs are based on SRAM technology and are customized by loading configuration data into internal memory cells and therefore it is very easy to re-program them an unlimited number of times. Updating the functionality of the FPGA only requires that the designer include a mechanism for updating the configuration bitstream.

The value of field upgradability is illustrated in Figure 5. A programmable ASSP, such as the Spartan-II family, allows a designer to gain market share by bringing them to market sooner than a stand-alone ASSP. The designer can also take advantage of the fact that the solution now allows them to upgrade their hardware and stay in the market-place longer, thus maximizing profitability.

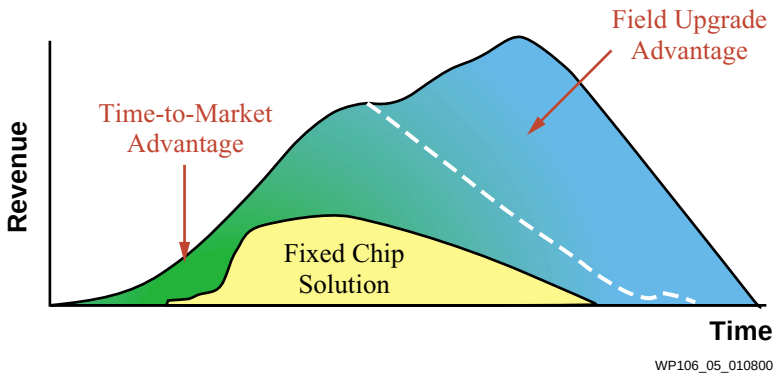

Figure 5: Field Upgradability Extends Value of Programmable ASSPs

Issues in Creating a Stand-alone ASSP

Vendors who create stand-alone ASSP devices must over-design their products to meet the requirements of a wide range of customers. They need to deal with a lot of issues to create a successful product, and all of these issues lead to increased cost, allowing programmable ASSPs, such as the Spartan-II FPGAs to compete effectively against some stand-alone ASSPs. A list of the various hurdles that an ASSP vendor faces today are briefly discussed here:

- **Choosing the Right ASSP**. The ASSP vendor must choose the right market segment to create their ASSP solution. It is difficult to target the right market and create a product that perfectly matches the market requirements. The cost of creating a solution for a wrong market, or for a market that has moved, is very expensive and has to be factored into the cost of all ASSPs shipped by the vendor. Understandably, a programmable ASSP does not have to deal with this issue. The cost of exploring new markets, the potential failure, and the eventual cost-adder are not applicable to the Spartan-II family.
- **Product Customization**. ASSP vendors face the challenge of creating one solution that has to successfully meet the demands of a wide range of customers. Most ASSP solutions fall into either of the two camps:
  - They are over-designed and result in increased pins, product cost, and feature set
  - Alternatively, they are under-designed and need a PLD to accommodate product customization

  The Spartan-II family can be customized to very specific needs, resulting in a cost-effective solution that also supports the exact functionality required.
- **Development Cost and Amortization.** Stand-alone ASSPs have high NRE and engineering costs. These costs are increasing with process technology migration. Mask charges for a 0.18 µm process can vary anywhere from $125K to $300K per set. This increases the cost of the ASSP significantly.

  The Spartan-II family has amortized cost by selling the devices as traditional PLDs. Their capability to act as a programmable ASSP does not increase their product cost. This is one of the fundamental reasons why Xilinx can provide a 32-bit, 33 MHz PCI solution for half the cost of stand-alone ASSPs of equivalent functionality.

The Spartan-II family is unaffected by the hurdles that an ASSP vendor needs to overcome and offers a cost-effective programmable ASSP solution; its inherent advantages extend the reach of the Spartan family to new levels and creates new opportunities for PLDs in the ASSP market.

Spartan-II ASSP Replacement Value

The Spartan-II family replaces and/or competes against three classes of ASSPs, they can be broadly classified as

- Feature-Replacement ASSPs
- Logic-Replacement ASSPs
- Value-added ASSPs

Feature-Replacement ASSPs

PLDs have been used as glue logic for the longest period of time and are now evolving into system-level integrators. This trend coupled with the adoption of aggressive process technologies push PLD architectures to accommodate features such as support for different I/O standards and voltages, DLLs, distributed and embedded memory blocks. The Spartan-II family supports 17 I/O standards and supports V_{CCIO} ranging from 1.8V to 5V. The Spartan-II family also supports four DLLs that can be used for many different applications.

Examples of "Feature Replacement ASSPs" and their approximate 100,000 unit volume pricing are shown in Table 1. All of these ASSPs can be replaced without any of the logic resources of the Spartan-II chip being consumed. The price of some of the Spartan-II chips are in some cases about the same price of the ASSP they replace. Therefore, the Spartan-II family allows the designer to get the gates for free.

Table 1: A Potential List of ASSPs that the Spartan-II Family Replaces by Virtue of its Features

Feature Replacement ASSPs	Price
32-bit SSTL-3 transceivers with 3-state outputs	$4.00
32-bit to 64-bit HSTL-to-LVTTL memory address latch	$6.00
32-bit LVTTL to GTL/GTL+ transcievers with live insertion	$6.00
High-speed CMOS digital PLLs	$1.00
High-speed programmable board skew clock buffer	$7.50
2K x 8 Dual-Port Static RAM	$2.00
64, 256, 512, 1K, 2K, 4K x 18 synchronous FIFOs	$7.00
Hot swap controller	$2.00

Note:

1. Pricing shown is approximate and for volumes of 100,000 units

Logic-replacement ASSPs

Logic-replacement ASSPs are categorized as those ASSPs that can be replaced by using the logic resources of a Spartan-II chip in combination with various IP cores. The Spartan-II family inherits unique features, density, extensive synthesizable IP portfolio and the cost structure to now effectively compete against this class of ASSPs.

Some ASIC vendors are pruning their ASSP product offering to focus on integrating larger systems-on-a-chip. This in turn allows the Spartan-II family to support these smaller density ASSP parts—a good example of this is the Reed-Solomon Encoder ASSP, which is used for error correction in many applications.

Examples of potential "Logic Replacement ASSPs" and their approximate 100,000 unit volume pricing are shown in Table . In all instances the Spartan-II solution combined with a synthesizable IP, cost effectively competes against these ASSPs and is priced under $10 in high volume.

Table 2: A Potential List of Logic Replacement ASSPs that the Spartan-II Family Supports

Logic Replacement ASSPs	Price
64-bit, 66 MHz PCI v2.2 bus master	$25.00
32-bit, 33 MHz CompactPCI® bus master hot swap friendly PCI interface chip	$15.00
32-bit, 33 MHz bus target chip	$12.00
32-bit, 33 MHz PCI master/slave controller	$14.00
32-bit, 33 MHz PCI target controller	$12.00
STS-12C/STS-3C POS/ATM SONET mapper	$120.00
PCI system controller for 64-bit MIPS CPUs with integrated SDRAM controller	$12.00
Advanced PCI system controller for 64-bit MIPS CPUs	$40.00
Secondary cache controller for the R4600/R4700	$15.00
Low-cost 8-port 10/100 fast ethernet switch controller	$28.00
High-speed microcontrollers are direct performance upgrades for the 8051	$8.00
256-channel HDLC controller	$60.00
Low-power version of DS80C320	$8.00
Multi-channel HDLC controller with 32-bit, 66 MHz PCI controller	$120.00
Block floating point 16 x 16 complex floating point multiplier	$300.00
Programmable FIR filter	$310.00
Standalone FFT processor	450.00
Integrated digitial switch	$12.00
HDLC protocol controller	$4.50
Multichannel ATM AAL1 SAR	90.00
Dual ADPCM transcoder	$4.00
Integrated PCM filter CODEC	$4.00
Viterbi with Reed-Solomon decoder	$25.00
Reed-Solomon forward error correction	$20.00
ALDC data compression	$12.00
DCLZ compression	$22.00
ISDN terminal adapter with HDLC controller	$10.00
Multichannel network unterface controller for HDLC	$60.00
Fast ethernet (100 Mbps) media access controllers (MAC)	$20.00

Note:

1. Pricing shown is approximate and for volumes of 100,000 units

Value-added ASSPs

Value-added ASSPs fall into either of two categories:

- ASSPs that take unique advantage of the Xilinx architecture like the ATM IMA devices from Applied Telecom. Applied Telecom is an AllianceCore partner and has customized their implementation of the IMA core to take advantage of the distributed memory in Spartan-II FPGAs to perform high-speed DSP functions. Their ATM IMA core solution is fully compliant with the ATM forum IMA specification. Spartan-II FPGAs allows Applied Telecom to sell their IMA solution at a very competitive price. The class of field-upgradable ASSPs and network processors also fall into this camp.

- ASSPs that serve emerging markets and markets that do not exist today, such as a PCI-X Master/Target controller.

Examples of "Value-added ASSPs", and their approximate 100,000 unit volume pricing are shown in Table 3. As mentioned previously, the Spartan-II solution combined with a synthesizable IP, cost effectively competes against these ASSPs and is priced under $10 in high volume.

Table 3: A Potential List of Value-added ASSPs that the Spartan-II Family Supports

Value Added ASSPs	Price
64-bit, 66 MHz PCI-X system controller	NA
Quad ATM IMA chip	$30.00
Octal ATM IMA chip	$50.00
ARC processor	NA

Note:

1. Pricing shown is approximate and for volumes of 100,000 units

The Spartan-II family services all three classifications of ASSPs very well and the number of ASSPs that it competes against is expected to increase significantly with time. Figure 6 highlights the ASSP replacement value message from a system-level perspective.

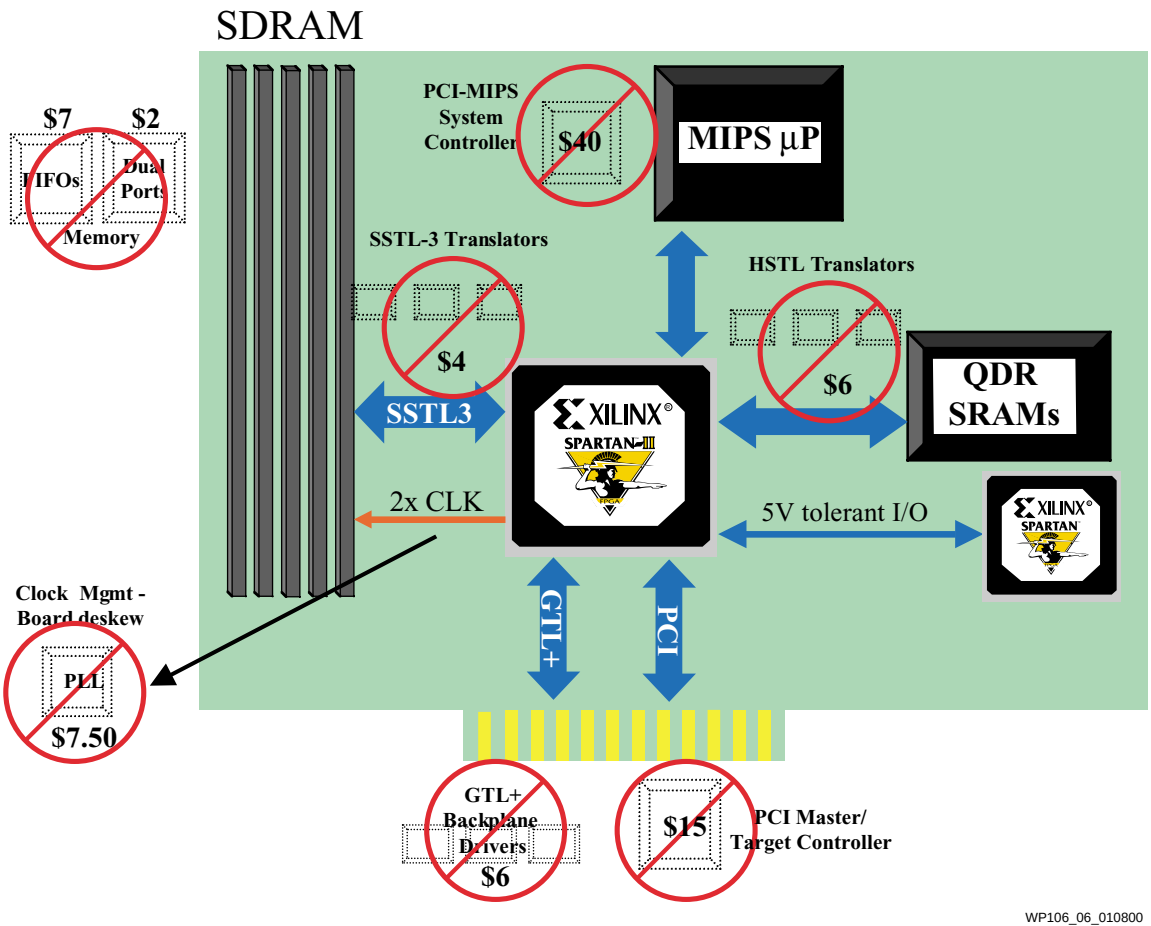

Figure 6: Spartan-II Family ASSP Replacement Value

Summary and Future Trends

This paper explored the dynamics in the ASIC/ASSP marketplace and the unique opportunities for the Spartan-II family, which will continue the trend set by earlier generations of FPGAs, in successfully penetrating the ASIC market. The Spartan-II family is also the first programmable logic family that is uniquely poised to penetrate the ASSP marketplace, due to its features and its cost effectiveness. The Spartan-II family will not compete against all ASSPs, but, it will hold its own in many applications and specifically in new emerging datacom, telecom, and consumer markets. The number of ASSPs that the Spartan-II family and its future derivatives compete against is expected to increase with time, enabling Xilinx to be a significant ASSP player.

References

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Revision History

Date	Version	Revision
01/10/00	1.0	Initial Xilinx release