

Using LVDS I/O

Introduction

Low Voltage Differential Signaling (LVDS) is a very popular and powerful high-speed interface in many system applications. When designing to comply with the IEEE standard specifications for LVDS in a data system and board design case, with the addition of an LVDS receiver mode driver in the ESD0, which distributes the need for external source termination in point-to-point applications, and with the choice of two different receiver modes and an external supply, ESD0 offers greater flexibility in the solution for LVDS designs on ESP32.

Table 2-16 lists all LVDS primitives that are available for ESD0 devices.

Table 2-16: Available LVDS I/O Primitives

| Input | Output | Driver | Driver | Is Inverted |
|----------------|----------------|----------------|----------------|-------------|
| lvds0_p0 | lvds0_n0 | lvds0_p0 | lvds0_n0 | lvds0_p0 |
| lvds0_p0_in | lvds0_n0_in | lvds0_p0_in | lvds0_n0_in | |
| lvds0_p0_oh | lvds0_n0_oh | lvds0_p0_oh | lvds0_n0_oh | |
| lvds0_p0_oh_in | lvds0_n0_oh_in | lvds0_p0_oh_in | lvds0_n0_oh_in | |
| lvds0_p0_oh_oh | lvds0_n0_oh_oh | lvds0_p0_oh_oh | lvds0_n0_oh_oh | |

The primitives include types are pre-existing LVDS primitives used in ESD0 and other designs. They are available in the ESD0 and are not required for ESD0 functionality applications.

• **lvds0_p0** = LVDS driver LVDS buffer

• **lvds0_n0** = LVDS driver LVDS buffer

There is no difference in the π characteristic of other voltage mode LVDS. It has three characteristics: more flexibility for circuit debugging, that is, an LVDS LVDS driver connected to the LVDS LVDS buffer in the same bank.

• **lvds0_p0_oh** = Open-drain mode LVDS buffer

Espressif provides a higher drive capability and voltage swing (P0-P0_oh), which makes it ideal for long distance LVDS links.

The support characteristics of the LVDS driver are not suitable for the specific case. The LVDS driver is used for applications that require higher drive capability in order to provide an LVDS signal to a wide line, the specifications of the receiver.

Creating an LVDS Input/Output Buffer

Figure 2-16 illustrates the LVDS input and clock buffer primitives shown in **Table 2-17**.

The pin names used in the case of these primitives ESD0 library primitives.

Table 2-17: LVDS Input and Clock Buffer Primitives

| LVDS Inputs | LVDS Clocks |
|----------------|-------------------|
| lvds0_p0_in | lvds0_p0_in_oh |
| lvds0_n0_in | lvds0_n0_in_oh |
| lvds0_p0_oh_in | lvds0_p0_oh_in_oh |
| lvds0_n0_oh_in | lvds0_n0_oh_in_oh |

Creating an LVCM Output Buffer

Figure 2.1.10 illustrates the LVCM output buffer pinlist (see

- `output_pin0_0`
- `output_pin0_1`
- `output_pin0val_0`
- `output_pin0val_1`

The pin names match the names of those used in the ICM library pinlist.



Figure 2.1.10: LVCM Output Buffer Pinlist

To create an LVCM output, instantiate the desired mode (CM, LCM, or threshold LVCM) output buffer. Notice that the ICM channels are included in the pinlist (e.g., I/P CM0 to I/P CM1), but users automatically use the appropriate pinlist as defined within the I channel.

LVCM Output ICM Examples

LVCM Initialization

```

icm = lvcm_output_pin0_0
pin0_val_0 = 1
o0_val = lvcm_out_0
o1_val = lvcm_out_1
icm_val = lvcm_val_0
    
```

Verilog Initialization

```

output_pin0_0[0] = 1; o0 = lvcm_out_0;
output_pin0_0[1] = 0; o1 = lvcm_out_1;
output_val_0[0]
    
```

Port Signals

`icm` = data input to the LVCM output buffer

`o0` = 0-bit data output

`o1` = 1-bit data output

Location Constraints

```

loc0 "lvcm_out_0" loc1 "icm";
    
```

LVCM Transmitter Termination

The threshold LVCM transmitter does not require any termination. **Table 2.5a** lists pinlists for that correspond to the threshold LVCM transmit mode drivers. Notice if LVCM transmit mode drivers are chosen, users must ensure and produce the proper (I/O, VLSI, I/O, compliance)/LVCM

signal. **Figure 3-88** illustrates a TriState I/O cell implementation as a based on the `IOBIO_000000000000` primitive.

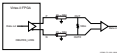


Figure 3-88: I/O Cell Implementation

Creating an I/O Cell Output 3-State Buffer

Figure 3-89 illustrates the I/O cell I/O buffer primitive:

- `data_in` [vector]
- `data_out` [vector]
- `tri_state` [vector]
- `tri_state` [vector]

The `tri_state` signals are the same as those used in the I/O cell library primitive.



Figure 3-89: I/O Cell I/O Buffer Primitive

To create an I/O cell I/O buffer output, instantiate the desired mode (P, N, or Bi) as described. I/O cell I/O buffer. Notice that the P and N channels are connected to the `data_in` and `data_out` signals, respectively, using the appropriate primitive as defined in the I/O cell library.

I/O Cell 3-State HDL Example

VHDL Instantiation

```

10. IOBIO_000000000000
    port map (
        O => IOBIO_000000000000,
        I => IOBIO_000000000000,
        O => IOBIO_000000000000,
        I => IOBIO_000000000000
    );

```

Verilog Implementation

```

    internal_data_in  = 0;
    internal_data_out = 0;
    internal_data_in  = 1;
    internal_data_out = 1;
    }
    }

```

Port Signals

- I = data input to the buffer register
- En = active control signal
- On = buffered data output
- Off = buffered data output

Location Constraints

```

    loc "max9024_0" loc "max9024_1";

```

LVDS 2-Bit Termination

The Verilog LVDS driver does not require any termination. [Table 2-6](#) lists pin assignments corresponding to the Verilog LVDS driver module. These drivers use two current sources, and they provide the proper (DR, TR, TR complement)/LVDS signal. The [Figure 2-6](#) illustrates a simple method for point-to-point LVDS driver-to-driver LVDS driver termination. Simply place a resistor across the required termination for the driver.

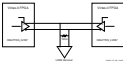


Figure 2-6 LVDS driver termination

Creating a Bidirectional LVDS Buffer

The bidirectional LVDS solution in the Verilog architecture is identical to the Verilog solution. These LVDSs are needed for point-to-point applications. An LVDS driver is not an OR/DR, TR complement implementation, but requires careful implementation of LV and TR before design rules. The procedure applies to the continuous library for bidirectional LVDS design for the Verilog LVDS driver module. Therefore, the following table details the rules:

- The LVDS driver LVDS pin connections for both I and O should meet the termination condition as the correct DR, TR and TR complement locations.
- The LVDS driver have the same connection as the following pin: clock, set, reset, enable, enable, feedback, output, and output clock enable.

- The output pins must be initialized with output mode values, and I/O pins require, in most, the I/OF statement for output values.
 - If I/O pins require mode, they must be initialized in the same state.
- Failure to follow these rules results in I/O errors in simulation.

WDL Initialization

```

I_0[0:15] = 0x000_0000
  (port map 1)
  O_0 = 0x00_0000
  O_1 = 0x00
  O2a = 0x00_000_00_00
  O_2 = 0x00_00_00
  O_3
  O4a[0:15] = 0x0
  (port map 1)
  O_4 = 0x00_0000
  O_5 = 0x00_000_000_000
  O_6
  O_7[0:15] = 0x0000_0000
  (port map 1)
  O_8 = 0x00_000_000_000
  O_9 = 0x00
  O10a = 0x00_000_00_00
  O_11 = 0x00
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L2T

Expanding Data Transport (L2T) is a new high-speed interface and protocol introduced by Espressif System/Espressif. L2T is a differential signaling based interface that is very similar to L2M. However, L2T is equipped with L2T header. These headers also have corresponding software operations as follows:

```
ESP2M_L2T_H  
ESP2M_L2T_H  
ESP2M_L2T_H  
ESP2M_L2T_H
```

L2T Implementation:

L2T implementation is the same as L2M in M2M2M as follows: all of the rules and guidelines in this section apply to L2M, L2B, and replace the L2M header with the corresponding L2T header. For more information on M2M2M electrical specifications, refer to the [Espressif Data Sheet](#).