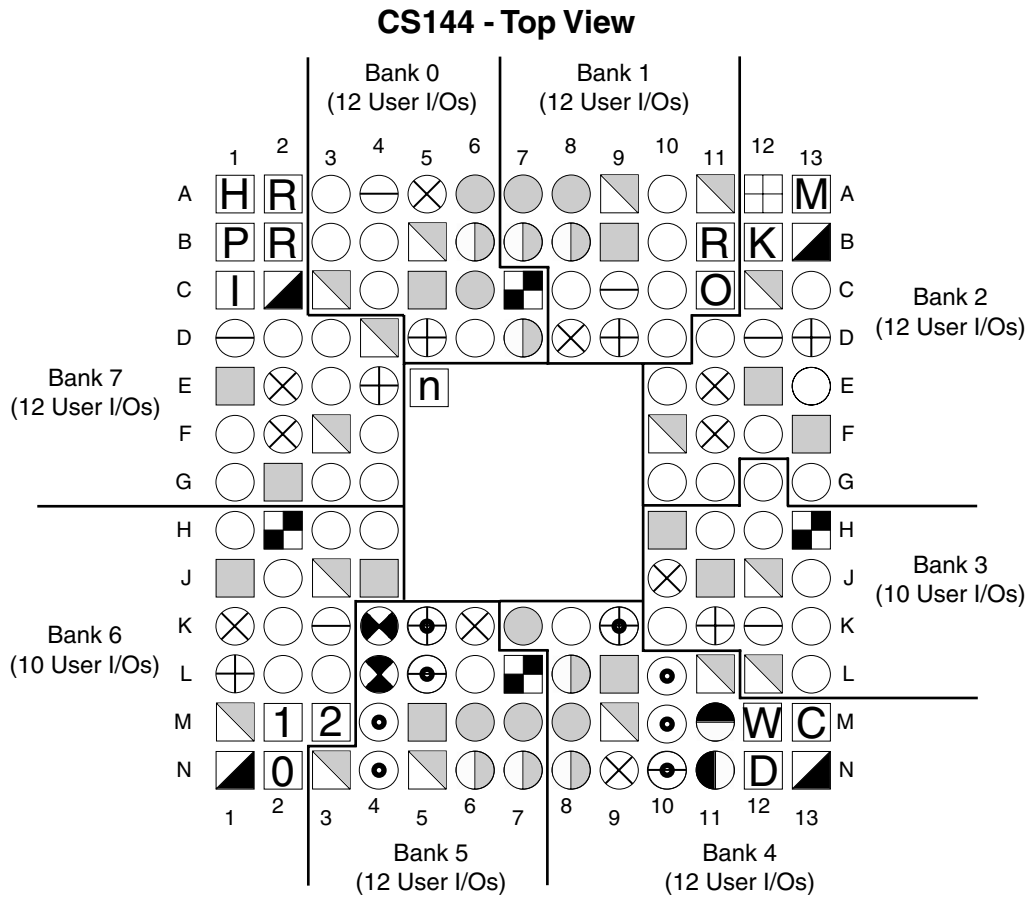


## Pinout Diagrams

This section contains pinout diagrams for the following Virtex-II packages:

- "CS144 Chip-Scale BGA Composite Pinout Diagram" on page 388
- "FG256 Fine-Pitch BGA Composite Pinout Diagram" on page 389
  - FG256 Bank Information
  - FG256 Dedicated Pins
- "FG456 Fine-Pitch BGA Composite Pinout Diagram" on page 393
  - FG456 Bank Information
  - FG456 Dedicated Pins
- "FG676 Fine-Pitch BGA Composite Pinout Diagram" on page 397
  - FG676 Bank Information
  - FG676 Dedicated Pins
- "BG575 Standard BGA Composite Pinout Diagram" on page 401
  - BG575 Bank Information
  - BG575 Dedicated Pins
- "BG728 Standard BGA Composite Pinout Diagram" on page 405
  - BG728 Bank Information
  - BG728 Dedicated Pins
- "FF896 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram" on page 409
  - FF896 Bank Information
  - FF896 Dedicated Pins
- "FF1152 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram" on page 413
  - FF1152 Bank Information
  - FF1152 Dedicated Pins
- "FF1517 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram" on page 417
  - FF1517 Bank Information
  - FF1517 Dedicated Pins
- "BF957 Flip-Chip BGA Composite Pinout Diagram" on page 421
  - BF957 Bank Information
  - BF957 Dedicated Pins
- "FG456 - FG676 Pinout Compatibility Diagram" on page 424
- "FF896 - FF1152 Pinout Compatibility Diagram" on page 425

CS144 Chip-Scale BGA Composite Pinout Diagram

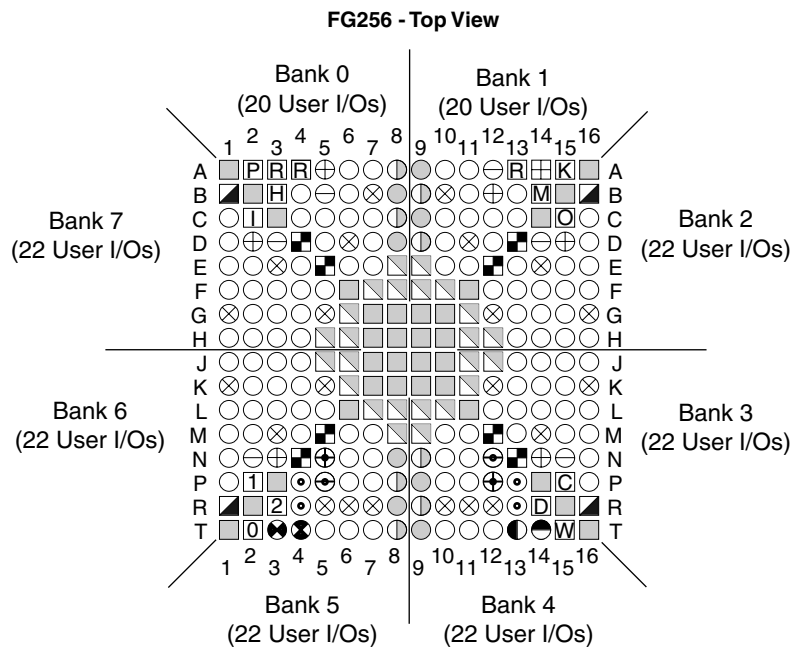


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	⊞ CCLK	⊞ VBATT
<u>Dual-Purpose Pins:</u>	⊞ PROG_B	⊞ RSVD
⊙ DIN/D0-D7	⊞ DONE	⊞ VCCO
⊗ CS_B	⊞ M2, M1, M0	⊞ VCCAUX
⊗ RDWR_B	⊞ HSWAP_EN	⊞ VCCINT
⊙ BUSY/DOUT	⊞ TCK	⊞ GND
⊙ INIT_B	⊞ TDI	⊞ NO CONNECT
⊙ GCLKx (P)	⊞ TDO	
⊙ GCLKx (S)	⊞ TMS	
⊖ VRP	⊞ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/VRP		
⊕ D3, D5/VRN		

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Figure 4-1: CS144 Chip-Scale BGA Composite Pinout Diagram

## FG256 Fine-Pitch BGA Composite Pinout Diagram

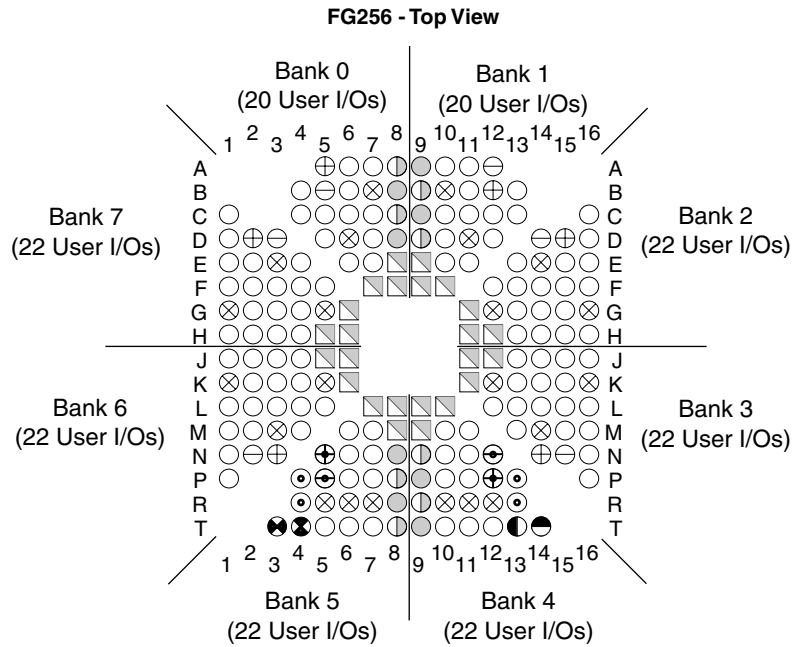


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	ⓐ CCLK	
<u>Dual-Purpose Pins:</u>	ⓑ PROG_B	
ⓐ DIN/D0-D7	ⓓ DONE	Ⓢ VBATT
ⓑ CS_B	Ⓜ M2, M1, M0	Ⓡ RSVD
ⓓ RDWR_B	ⓗ HSWAP_EN	Ⓥ VCCO
Ⓢ BUSY/DOUT	Ⓚ TCK	Ⓦ VCCAUX
Ⓡ INIT_B	Ⓛ TDI	Ⓨ VCCINT
Ⓥ GCLKx (P)	ⓐ TDO	Ⓩ GND
Ⓩ GCLKx (S)	Ⓜ TMS	Ⓨ NO CONNECT
Ⓡ VRP	Ⓦ PWRDWN_B	
Ⓡ VRN		
Ⓢ VREF		
<u>Triple-Purpose Pins:</u>		
Ⓢ D2, D4/VRP		
Ⓡ D3, D5/VRN		

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Figure 4-2: FG256 Fine-Pitch BGA Composite Pinout Diagram

FG256 Bank Information



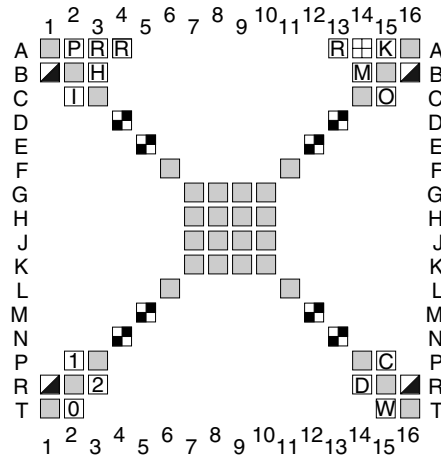
User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<u>Dual-Purpose Pins:</u>		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▣ VCCO
⊖ BUSY/DOUT		
⊖ INIT_B		
⊙ GCLKx (P)		
⊙ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊖ D2, D4/VRP		
⊕ D3, D5/VRN		

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Figure 4-3: FG256 Bank Information

FG256 Dedicated Pins

FG256 - Top View



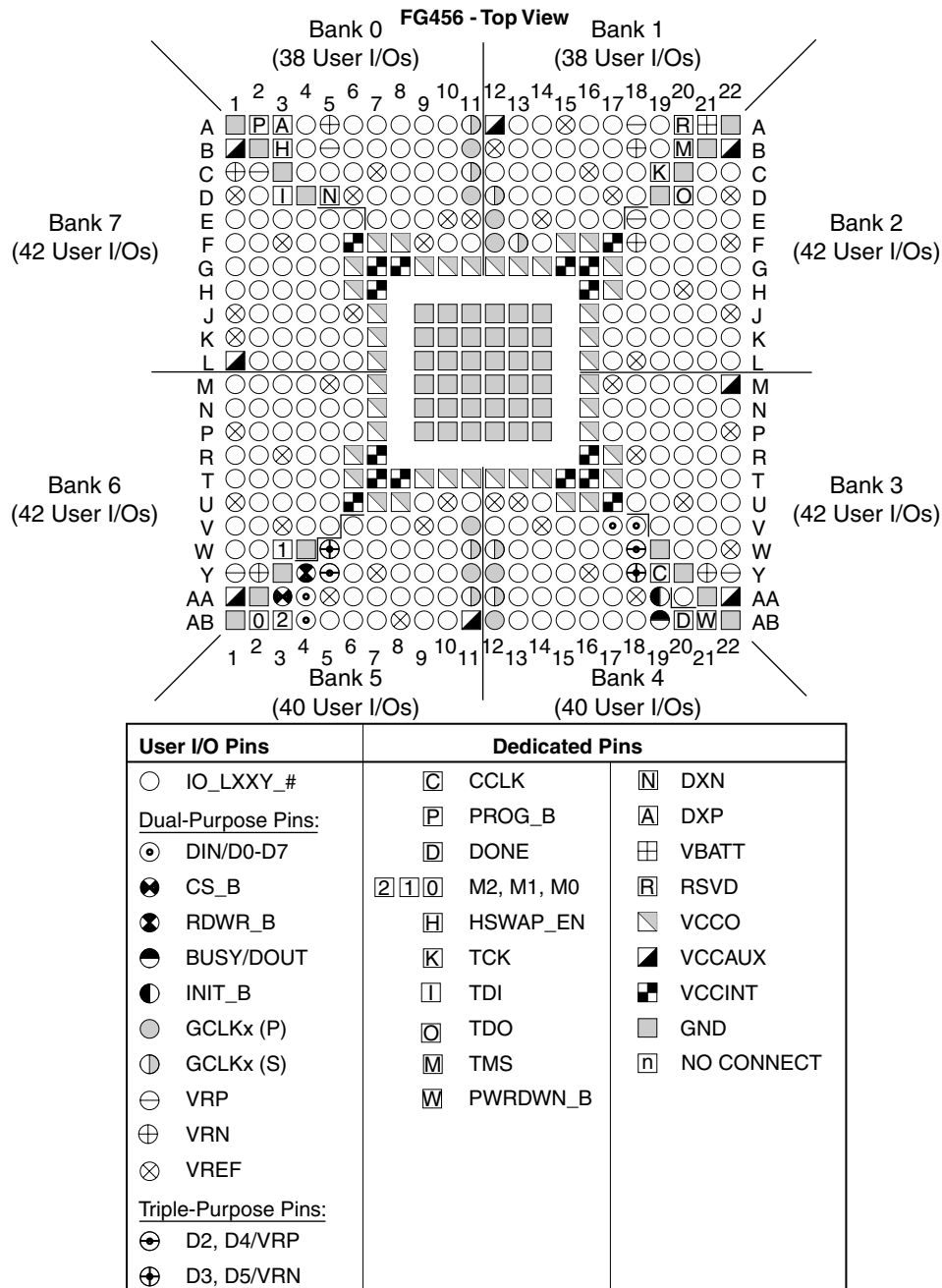
User I/O Pins	Dedicated Pins	
	<ul style="list-style-type: none"> <li> CCLK</li> <li> PROG_B</li> <li> DONE</li> <li> M2, M1, M0</li> <li> HSWAP_EN</li> <li> TCK</li> <li> TDI</li> <li> TDO</li> <li> TMS</li> <li> PWRDWN_B</li> </ul>	<ul style="list-style-type: none"> <li> VBATT</li> <li> RSVD</li> <li> VCCAUX</li> <li> VCCINT</li> <li> GND</li> <li> NO CONNECT</li> </ul>

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Figure 4-4: FG256 Dedicated Pins



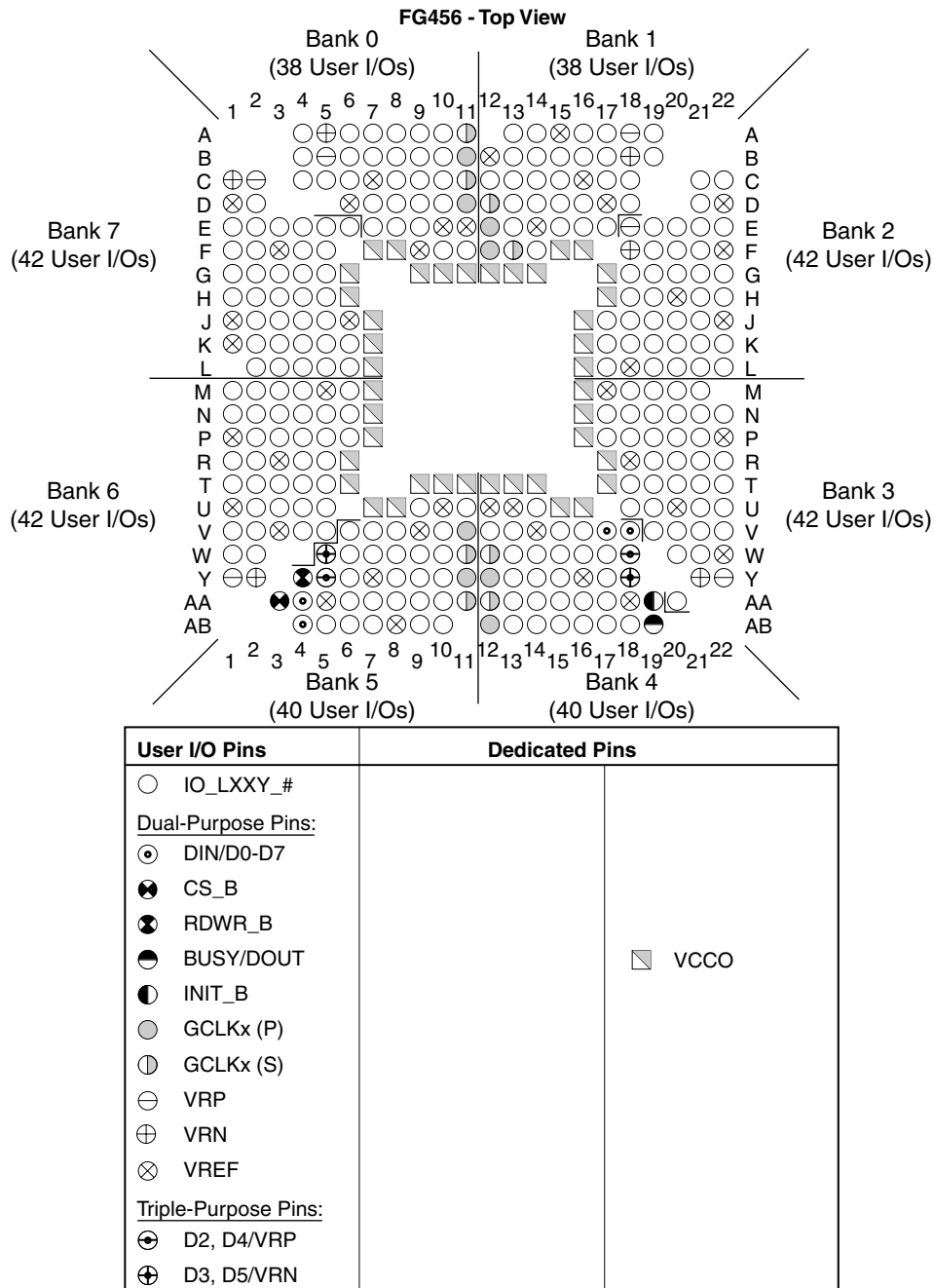
## FG456 Fine-Pitch BGA Composite Pinout Diagram



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Figure 4-5: FG456 Fine-Pitch BGA Composite Pinout Diagram

FG456 Bank Information

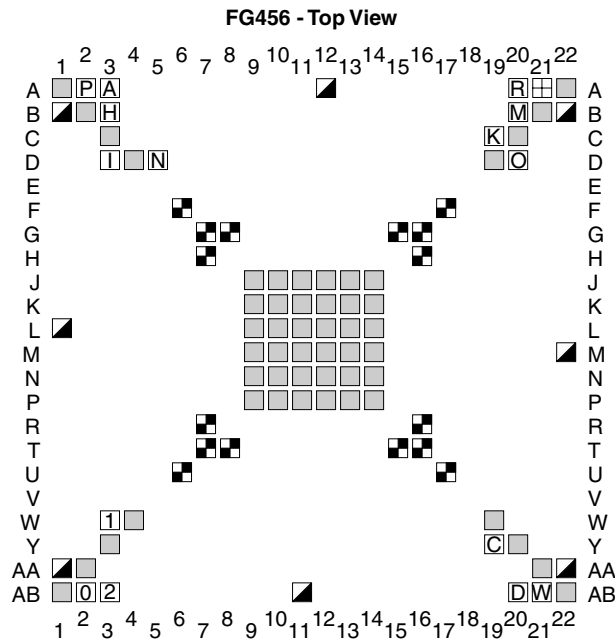


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Figure 4-6: FG456 Bank Information



FG456 Dedicated Pins



4

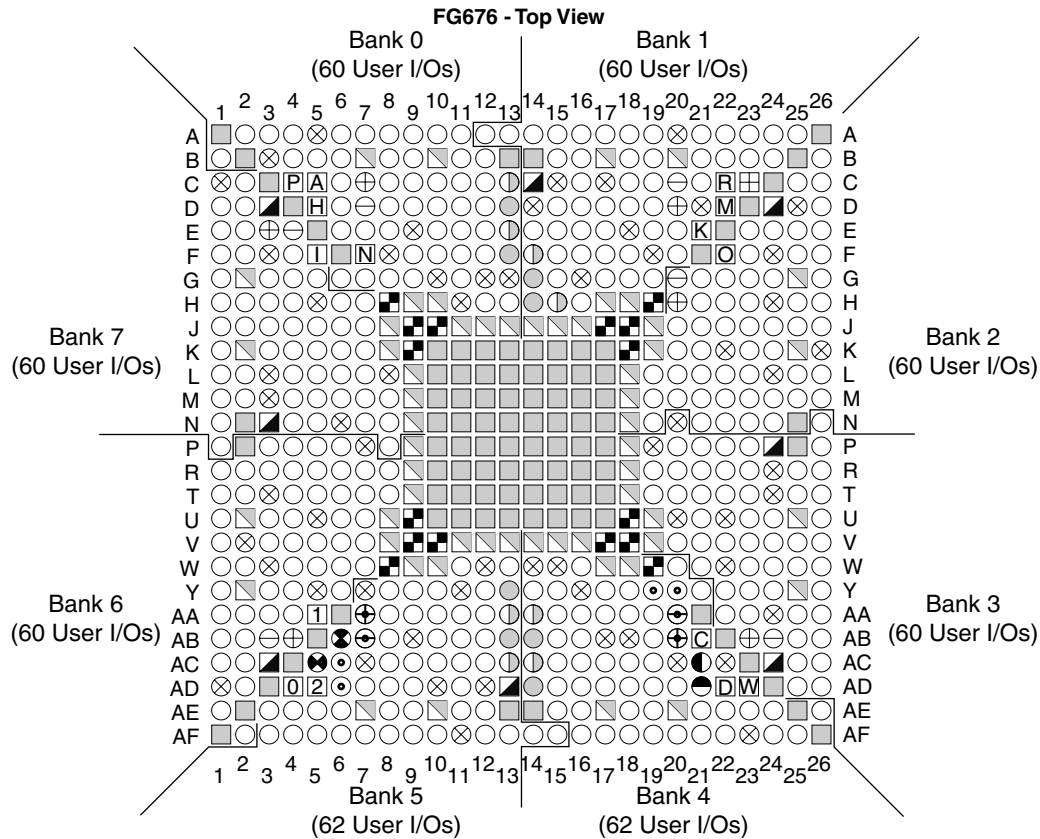
User I/O Pins	Dedicated Pins	
	<ul style="list-style-type: none"> <li><span style="border: 1px solid black; padding: 2px;">C</span> CCLK</li> <li><span style="border: 1px solid black; padding: 2px;">P</span> PROG_B</li> <li><span style="border: 1px solid black; padding: 2px;">D</span> DONE</li> <li><span style="border: 1px solid black; padding: 2px;">2</span><span style="border: 1px solid black; padding: 2px;">1</span><span style="border: 1px solid black; padding: 2px;">0</span> M2, M1, M0</li> <li><span style="border: 1px solid black; padding: 2px;">H</span> HSWAP_EN</li> <li><span style="border: 1px solid black; padding: 2px;">K</span> TCK</li> <li><span style="border: 1px solid black; padding: 2px;">I</span> TDI</li> <li><span style="border: 1px solid black; padding: 2px;">O</span> TDO</li> <li><span style="border: 1px solid black; padding: 2px;">M</span> TMS</li> <li><span style="border: 1px solid black; padding: 2px;">W</span> PWRDWN_B</li> </ul>	<ul style="list-style-type: none"> <li><span style="border: 1px solid black; padding: 2px;">N</span> DXN</li> <li><span style="border: 1px solid black; padding: 2px;">A</span> DXP</li> <li><span style="border: 1px solid black; padding: 2px;">+</span> VBATT</li> <li><span style="border: 1px solid black; padding: 2px;">R</span> RSVD</li> <li><span style="border: 1px solid black; padding: 2px;">▀</span> VCCAUX</li> <li><span style="border: 1px solid black; padding: 2px;">■</span> VCCINT</li> <li><span style="border: 1px solid black; padding: 2px;">□</span> GND</li> <li><span style="border: 1px solid black; padding: 2px;">n</span> NO CONNECT</li> </ul>

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Figure 4-7: FG456 Dedicated Pins



## FG676 Fine-Pitch BGA Composite Pinout Diagram



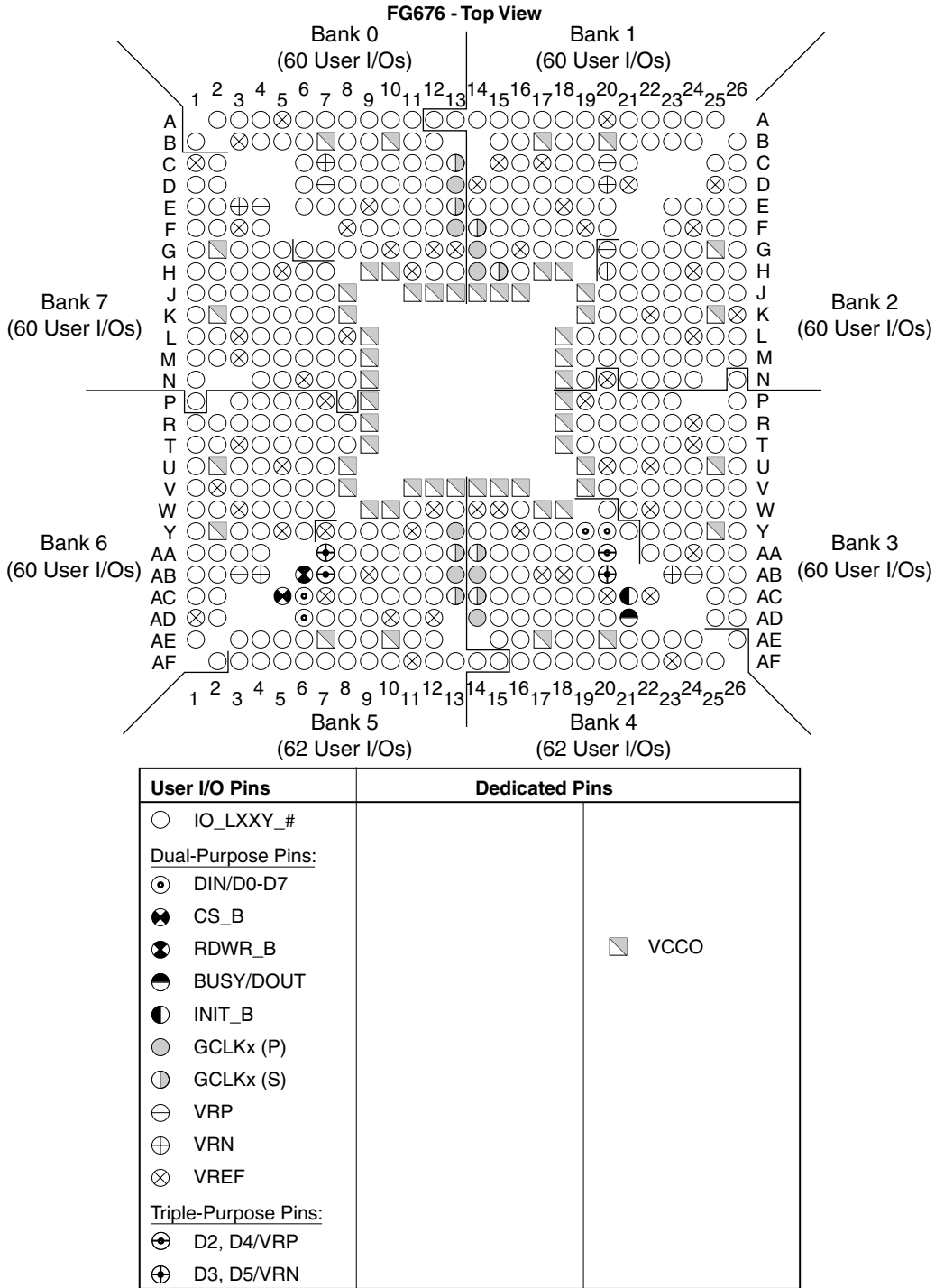
4

User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	Ⓢ CCLK	Ⓝ DXN
<u>Dual-Purpose Pins:</u>	Ⓟ PROG_B	Ⓜ DXP
⊙ DIN/D0-D7	Ⓞ DONE	Ⓜ VBATT
⊗ CS_B	Ⓜ M2, M1, M0	Ⓜ RSVD
⊗ RDWR_B	Ⓜ HSWAP_EN	Ⓜ VCCO
⊗ BUSY/DOUT	Ⓜ TCK	Ⓜ VCCAUX
⊗ INIT_B	Ⓜ TDI	Ⓜ VCCINT
⊗ GCLKx (P)	Ⓜ TDO	Ⓜ GND
⊗ GCLKx (S)	Ⓜ TMS	Ⓜ NO CONNECT
⊗ VRP	Ⓜ PWRDWN_B	
⊗ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊗ D2, D4/VRP		
⊗ D3, D5/VRN		

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Figure 4-8: FG676 Fine-Pitch BGA Composite Pinout Diagram

FG676 Bank Information

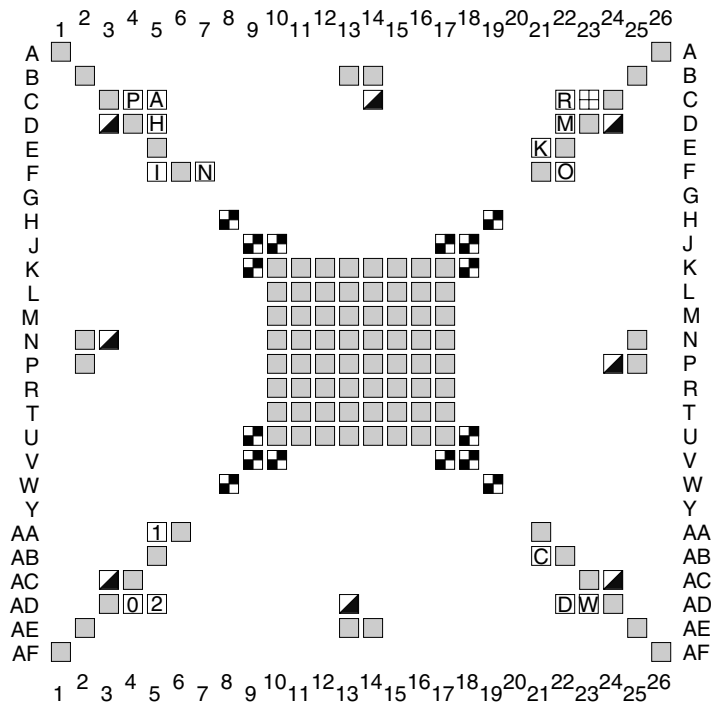


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Figure 4-9: FG676 Bank Information

FG676 Dedicated Pins

FG676 - Top View



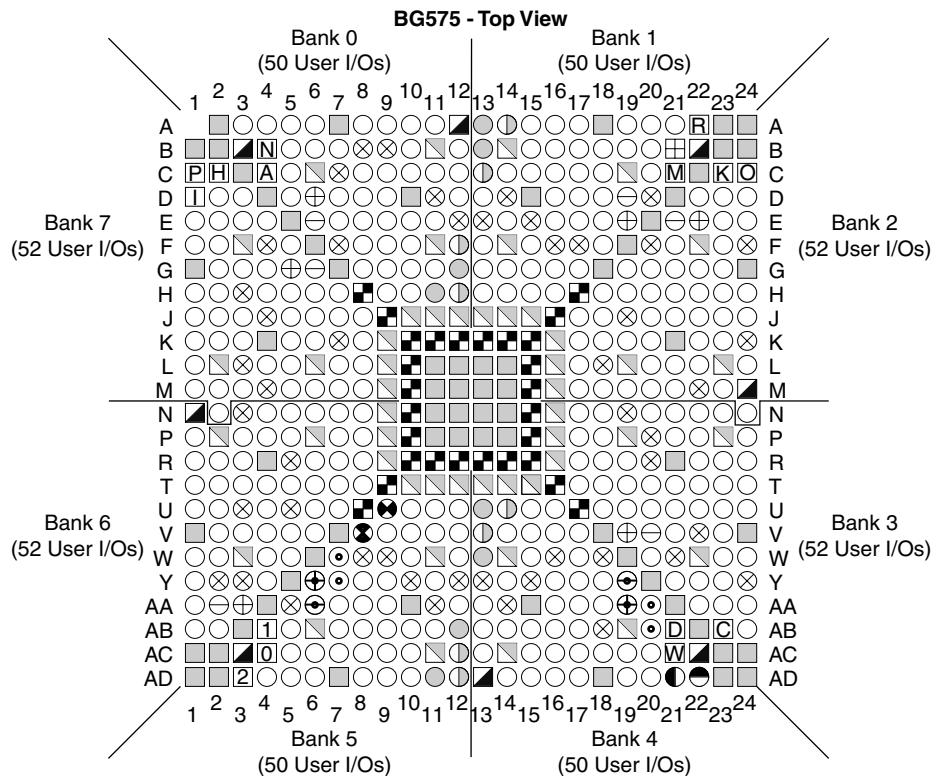
User I/O Pins	Dedicated Pins	
	ⓐ CCLK	Ⓝ DXN
	Ⓟ PROG_B	Ⓐ DXP
	ⓓ DONE	⊕ VBATT
	②①① M2, M1, M0	Ⓡ RSVD
	ⓗ HSWAP_EN	▣ VCCAUX
	Ⓚ TCK	■ VCCINT
	Ⓦ TDI	□ GND
	Ⓞ TDO	◻ NO CONNECT
	Ⓜ TMS	
	Ⓦ PWRDWN_B	

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Figure 4-10: FG676 Dedicated Pins



## BG575 Standard BGA Composite Pinout Diagram

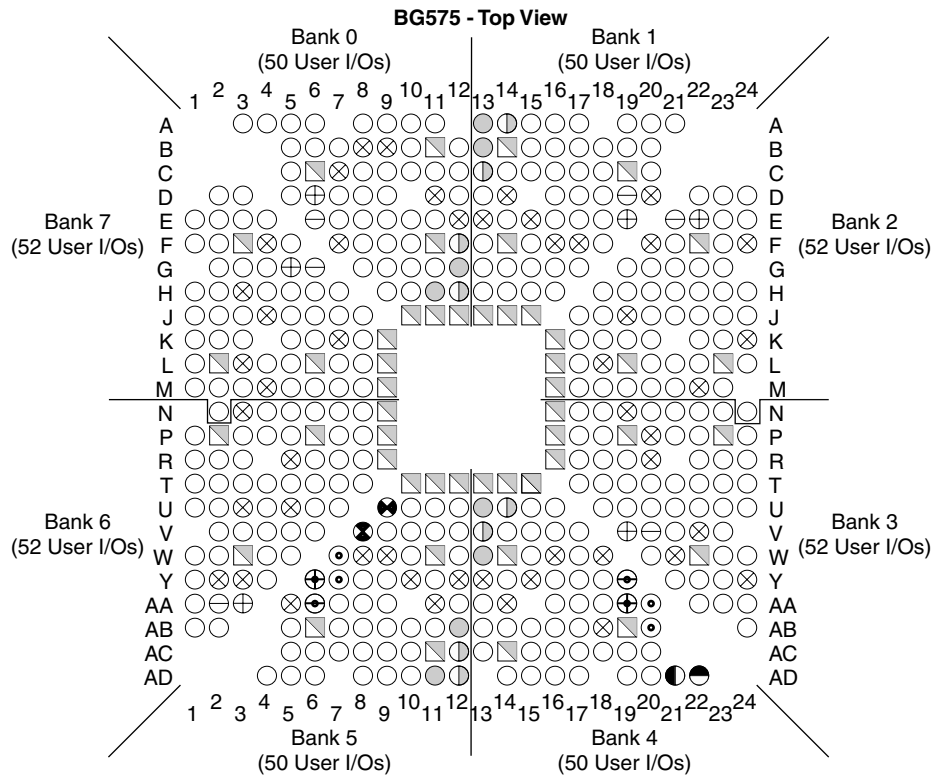


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	ⓐ CCLK	Ⓝ DXN
<u>Dual-Purpose Pins:</u>	ⓑ PROG_B	Ⓞ DXP
⊕ DIN/D0-D7	ⓓ DONE	Ⓢ VBATT
⊗ CS_B	Ⓜ2 Ⓜ1 Ⓜ0 M2, M1, M0	Ⓡ RSVD
⊗ RDWR_B	ⓗ HSWAP_EN	Ⓥ VCCO
⊖ BUSY/DOUT	Ⓚ TCK	Ⓦ VCCAUX
⊙ INIT_B	Ⓛ TDI	Ⓧ VCCINT
⊙ GCLKx (P)	Ⓛ TDO	Ⓧ GND
⊙ GCLKx (S)	Ⓜ TMS	Ⓨ NO CONNECT
⊖ VRP	Ⓦ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/VRP		
⊕ D3, D5/VRN		

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Figure 4-11: BG575 Standard BGA Composite Pinout Diagram

BG575 Bank Information



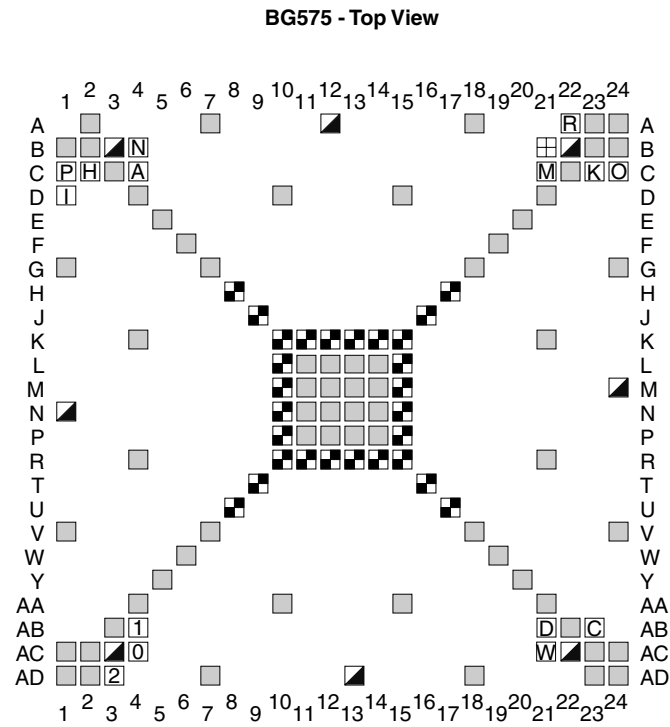
User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<u>Dual-Purpose Pins:</u>		
⊕ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▣ VCCO
● BUSY/DOUT		
◐ INIT_B		
● GCLKx (P)		
◐ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/VRP		
⊕ D3, D5/VRN		

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Figure 4-12: BG575 Bank Information



BG575 Dedicated Pins



4

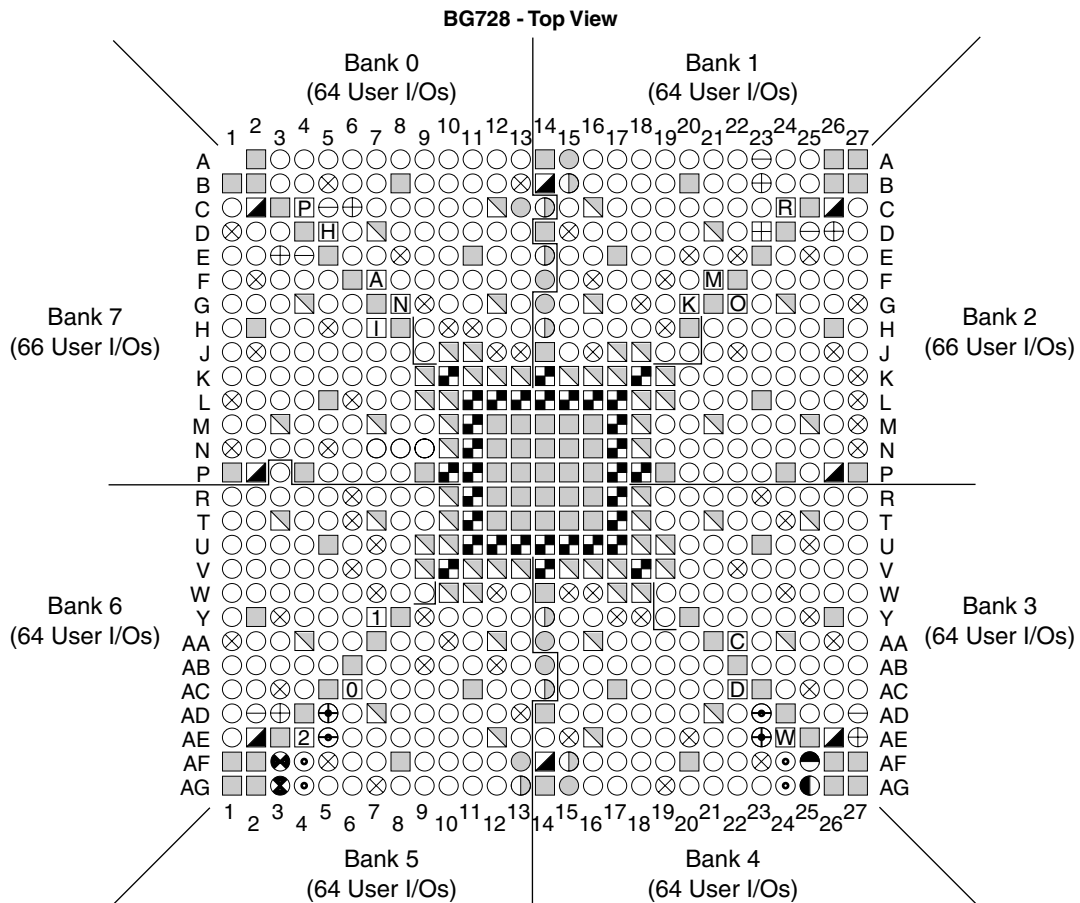
User I/O Pins	Dedicated Pins	
	<ul style="list-style-type: none"> <li><b>C</b> CCLK</li> <li><b>P</b> PROG_B</li> <li><b>D</b> DONE</li> <li><b>2 1 0</b> M2, M1, M0</li> <li><b>H</b> HSWAP_EN</li> <li><b>K</b> TCK</li> <li><b>I</b> TDI</li> <li><b>O</b> TDO</li> <li><b>M</b> TMS</li> <li><b>W</b> PWRDWN_B</li> </ul>	<ul style="list-style-type: none"> <li><b>N</b> DXN</li> <li><b>A</b> DXP</li> <li><b>V</b> VBATT</li> <li><b>R</b> RSVD</li> <li><b>V</b> VCCAUX</li> <li><b>I</b> VCCINT</li> <li><b>G</b> GND</li> <li><b>n</b> NO CONNECT</li> </ul>

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Figure 4-13: BG575 Dedicated Pins



## BG728 Standard BGA Composite Pinout Diagram



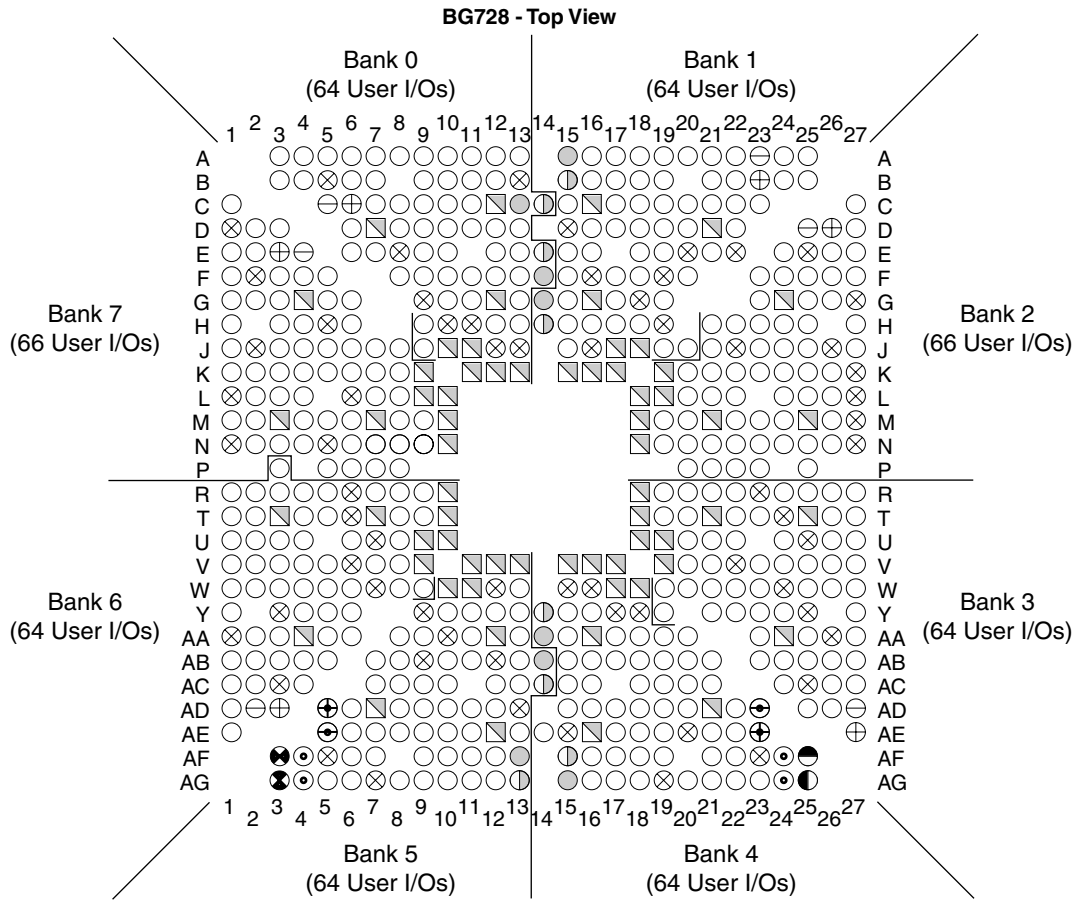
4

User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	Ⓢ CCLK	Ⓝ DXN
<u>Dual-Purpose Pins:</u>	Ⓟ PROG_B	Ⓜ DXP
⊙ DIN/D0-D7	Ⓣ DONE	Ⓜ VBATT
⊗ CS_B	Ⓜ M2, M1, M0	Ⓝ RSVD
⊗ RDWR_B	Ⓜ HSWAP_EN	Ⓝ VCCO
⊗ BUSY/DOUT	Ⓜ TCK	Ⓜ VCCAUX
⊗ INIT_B	Ⓜ TDI	Ⓜ VCCINT
⊗ GCLKx (P)	Ⓜ TDO	Ⓜ GND
⊗ GCLKx (S)	Ⓜ TMS	Ⓜ NO CONNECT
⊗ VRP	Ⓜ PWRDWN_B	
⊗ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊗ D2, D4/VRP		
⊗ D3, D5/VRN		

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Figure 4-14: BG728 Standard BGA Composite Pinout Diagram

BG728 Bank Information

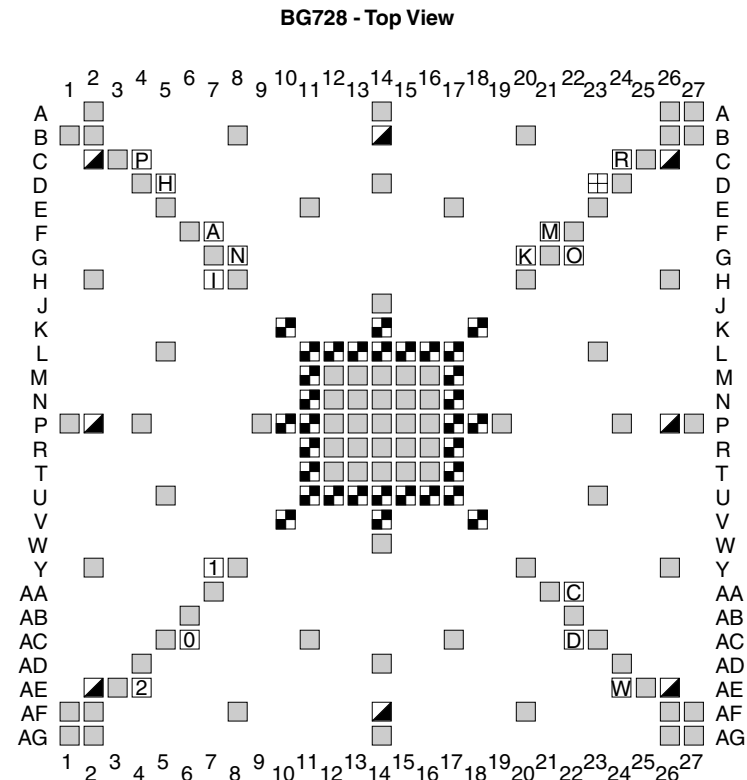


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<u>Dual-Purpose Pins:</u>		
⊙ DIN/D0-D7		
⊗ CS_B		◻ VCCO
⊗ RDWR_B		
● BUSY/DOUT		
◐ INIT_B		
● GCLKx (P)		
◐ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/VRP		
⊕ D3, D5/VRN		

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Figure 4-15: BG728 Bank Information

BG728 Dedicated Pins



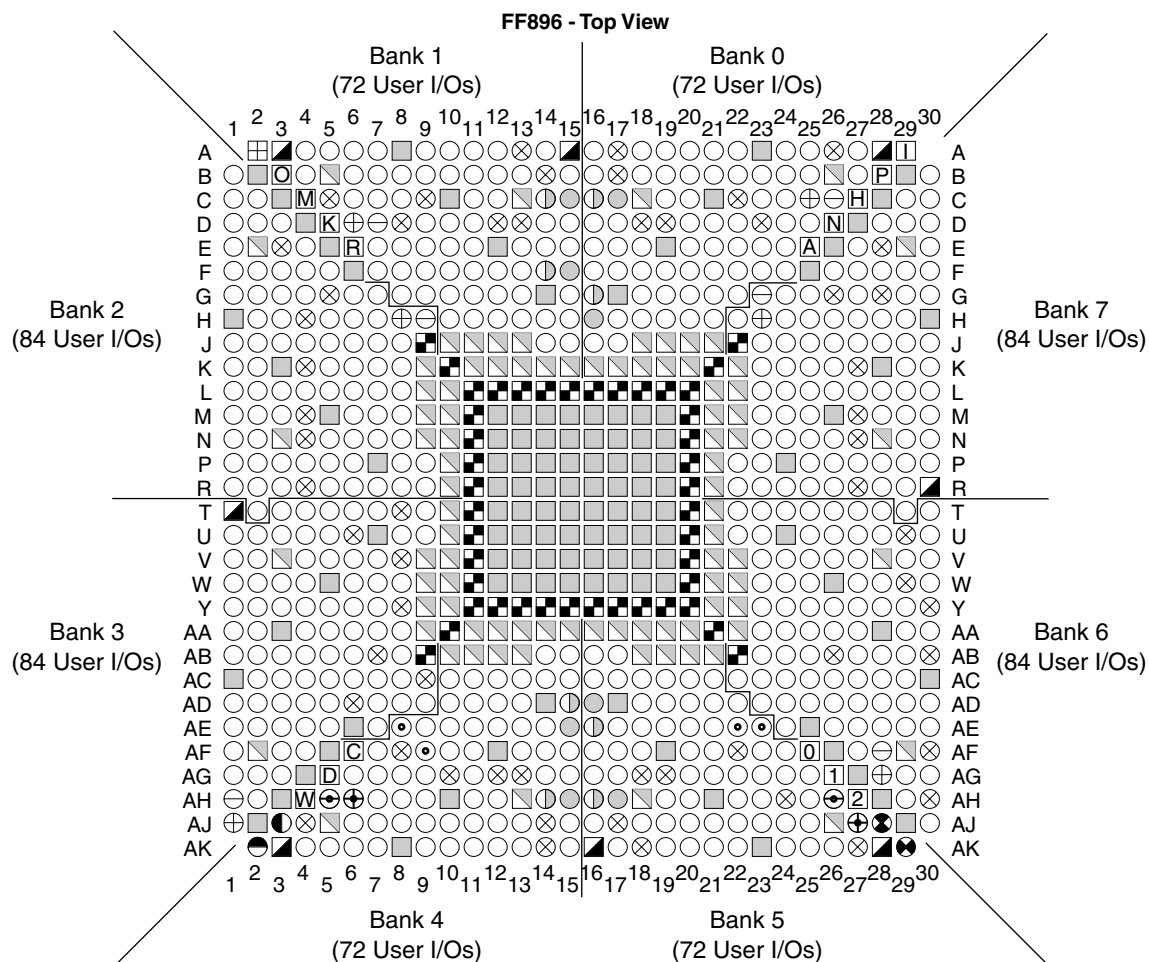
User I/O Pins	Dedicated Pins	
	ⓐ CCLK	Ⓝ DXN
	Ⓟ PROG_B	ⓐ DXP
	ⓓ DONE	Ⓜ VBATT
	ⓂⓂⓄ M2, M1, M0	Ⓡ RSVD
	ⓗ HSWAP_EN	⚡ VCCAUX
	Ⓚ TCK	⚫ VCCINT
	Ⓜ TDI	Ⓞ GND
	Ⓞ TDO	Ⓝ NO CONNECT
	Ⓜ TMS	
	Ⓜ PWRDWN_B	

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Figure 4-16: BG728 Dedicated Pins



## FF896 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram



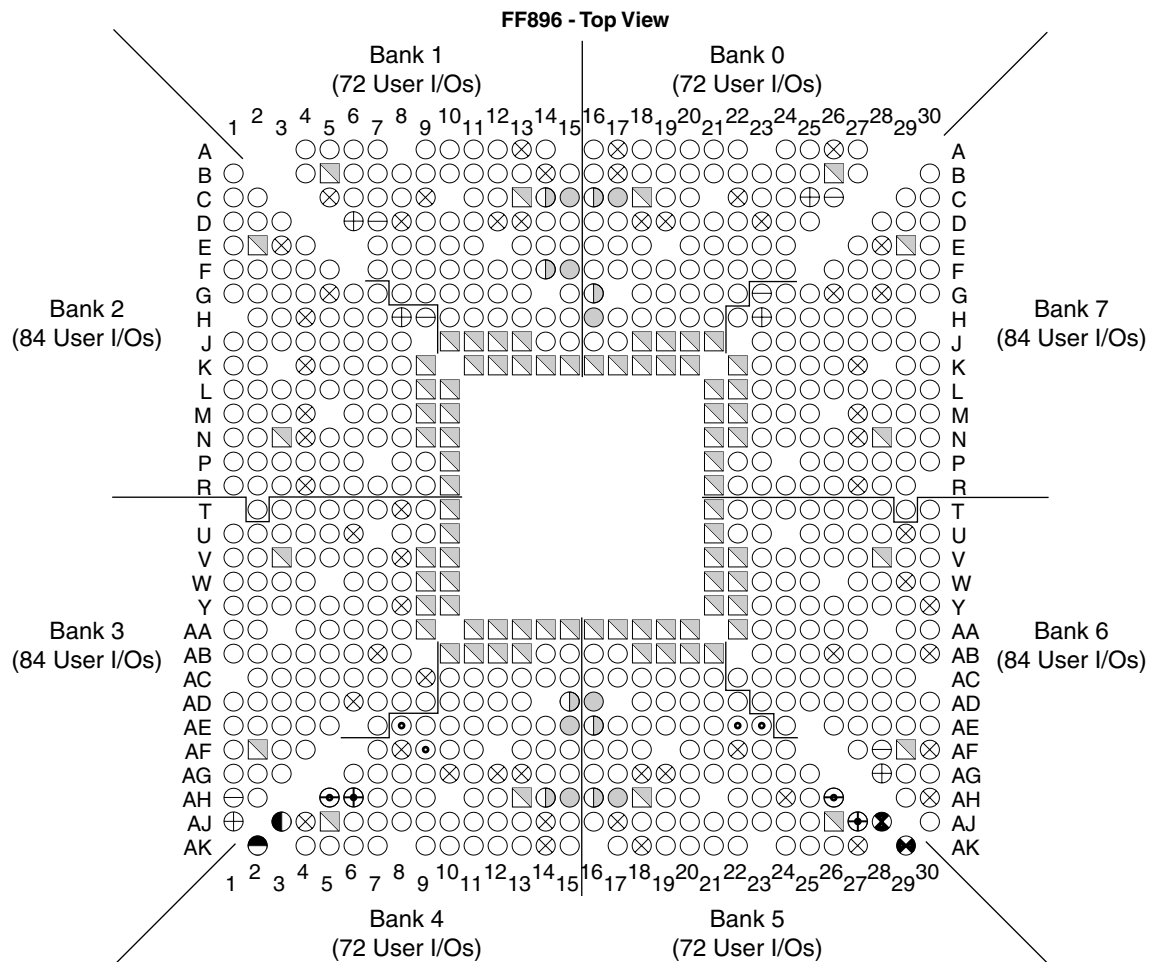
4

User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	ⓐ CCLK	Ⓝ DXN
<u>Dual-Purpose Pins:</u>	Ⓟ PROG_B	ⓐ DXP
⊙ DIN/D0-D7	ⓓ DONE	⊞ VBATT
⊗ CS_B	Ⓜ M2, M1, M0	Ⓡ RSVD
⊗ RDWR_B	ⓗ HSWAP_EN	⊞ VCCO
● BUSY/DOUT	Ⓚ TCK	⬛ VCCAUX
● INIT_B	Ⓛ TDI	⬛ VCCINT
● GCLKx (P)	ⓐ TDO	■ GND
Ⓛ GCLKx (S)	Ⓜ TMS	Ⓝ NO CONNECT
⊖ VRP	Ⓦ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2,D4/VRP		
⊕ D3,D5/VRN		

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**Figure 4-17: FF896 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram**

FF896 Bank Information



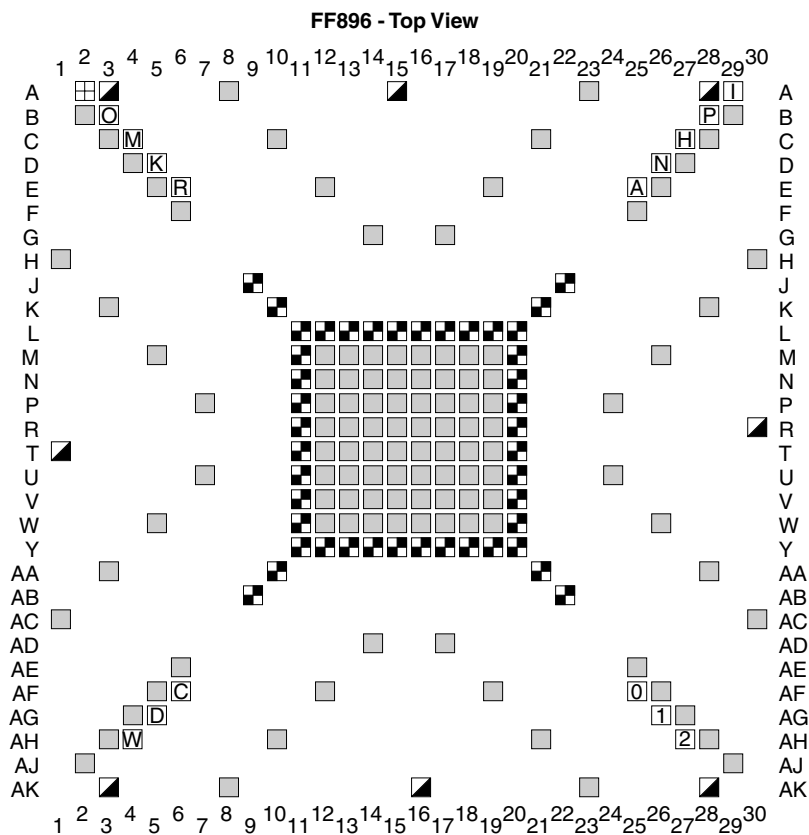
User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<u>Dual-Purpose Pins:</u>		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▣ VCCO
● BUSY/DOUT		
● INIT_B		
● GCLKx (P)		
⊙ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊖⊕ D2, D4/VRP		
⊕⊗ D3, D5/VRN		

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Figure 4-18: FF896 Bank Information



### FF896 Dedicated Pins



4

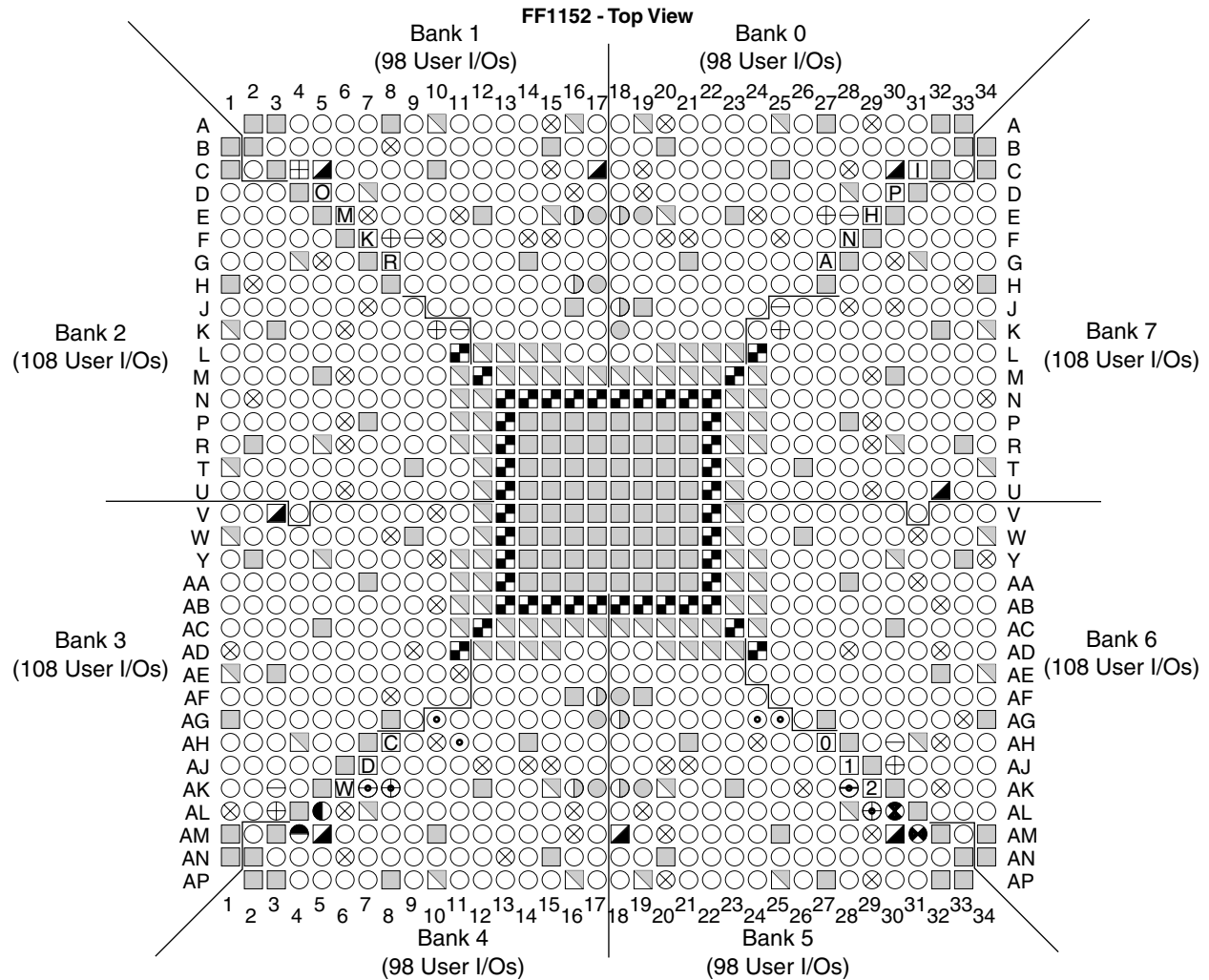
User I/O Pins	Dedicated Pins	
	Ⓒ CCLK	⒩ DXN
	Ⓟ PROG_B	Ⓐ DXP
	Ⓛ DONE	⊕ VBATT
	ⓂⓁⓂⓂ M2, M1, M0	Ⓡ RSVD
	ⓗ HSWAP_EN	⚡ VCCAUX
	Ⓚ TCK	⚫ VCCINT
	Ⓜ TDI	Ⓛ GND
	Ⓞ TDO	Ⓜ NO CONNECT
	Ⓜ TMS	
	Ⓦ PWRDWN_B	

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Figure 4-19: FF896 Dedicated Pins



## FF1152 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram

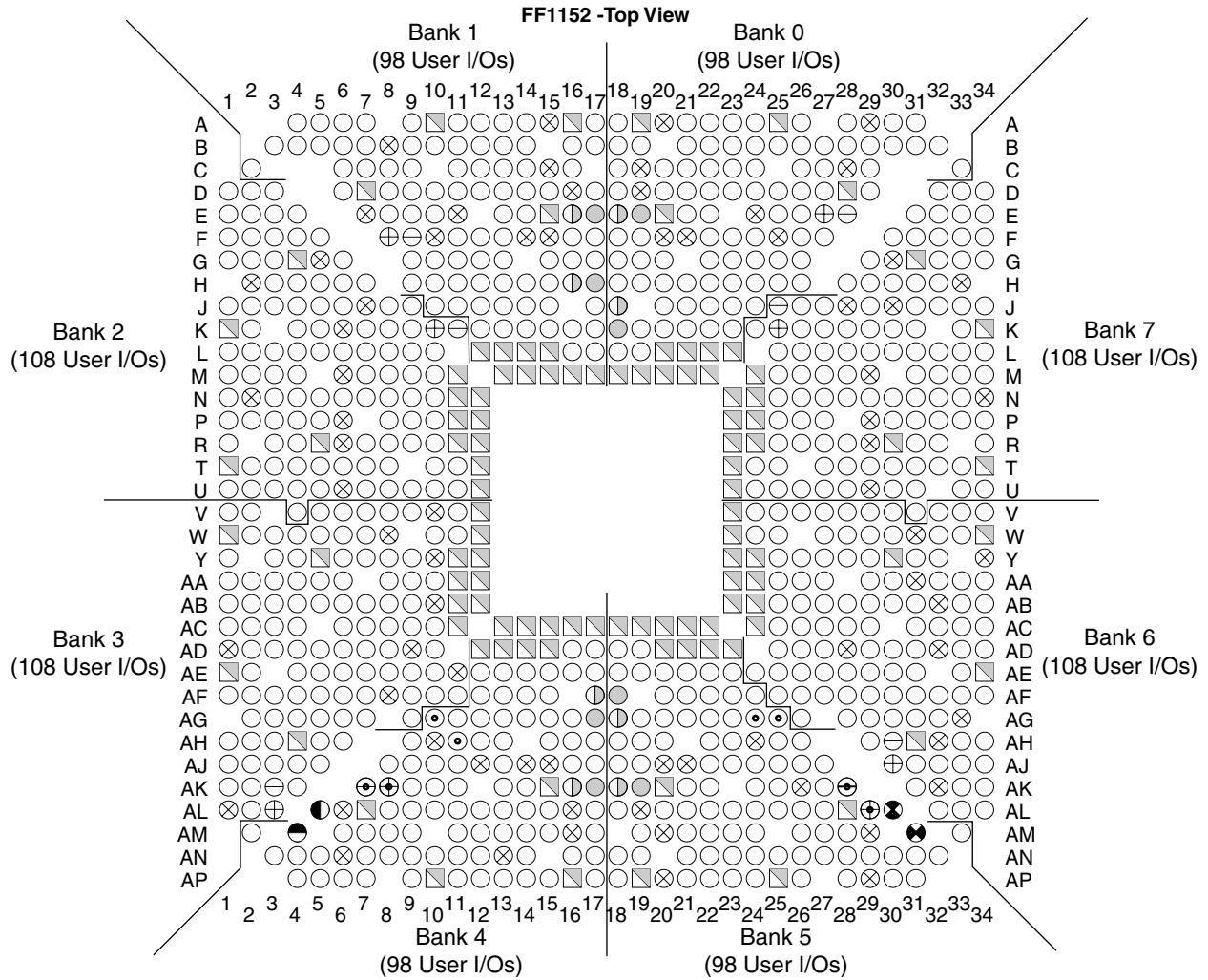


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	Ⓒ CCLK	⒩ DXN
<u>Dual-Purpose Pins:</u>	⒫ PROG_B	Ⓐ DXP
⊙ DIN/D0-D7	Ⓓ DONE	⊞ VBATT
⊗ CS_B	Ⓜ M2, M1, M0	Ⓔ RSVD
⊗ RDWR_B	Ⓗ HSWAP_EN	⊞ VCCO
⊙ BUSY/DOUT	Ⓖ TCK	⬛ VCCAUX
⊙ INIT_B	Ⓛ TDI	⬛ VCCINT
⊙ GCLKx (P)	Ⓞ TDO	⬜ GND
⊙ GCLKx (S)	Ⓜ TMS	Ⓛ NO CONNECT
⊖ VRP	Ⓦ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/VRP		
⊕ D3, D5/VRN		

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Figure 4-20: FF1152 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram

FF1152 Bank Information

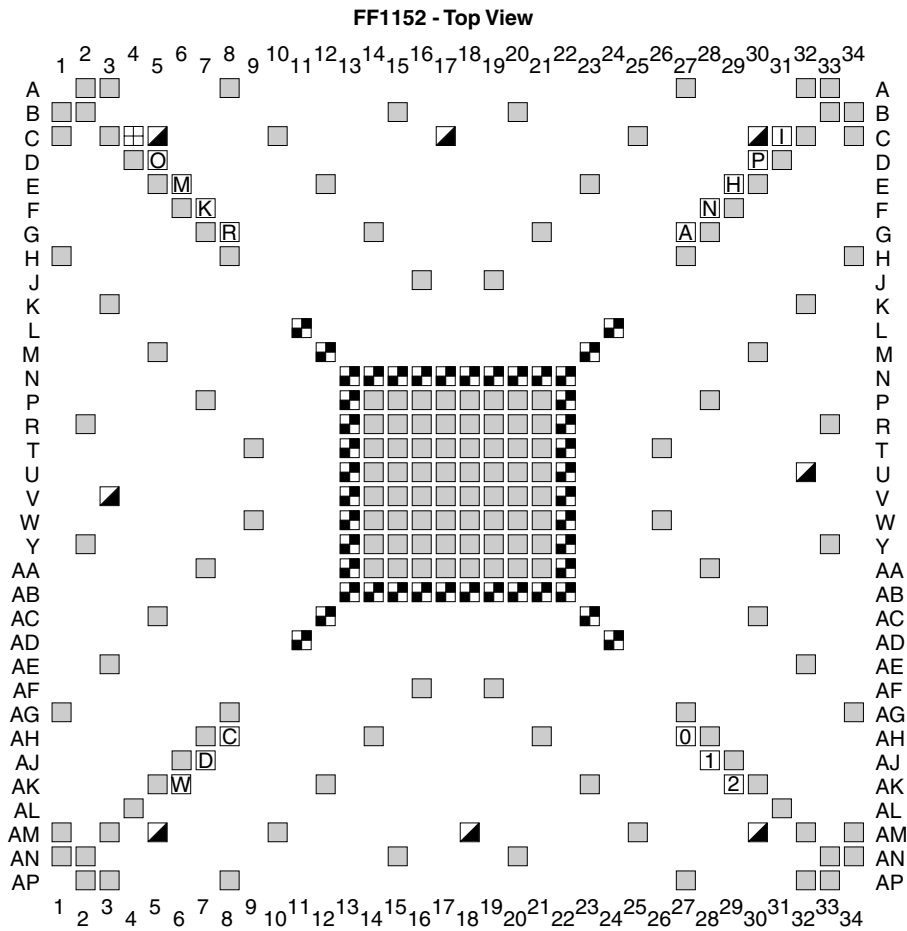


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<u>Dual-Purpose Pins:</u>		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		
● BUSY/DOUT		
◐ INIT_B		
● GCLKx (P)		
◐ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/VRP		
⊕ D3, D5/VRN		
		◐ VCCO

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Figure 4-21: FF1152 Bank Information

### FF1152 Dedicated Pins



4

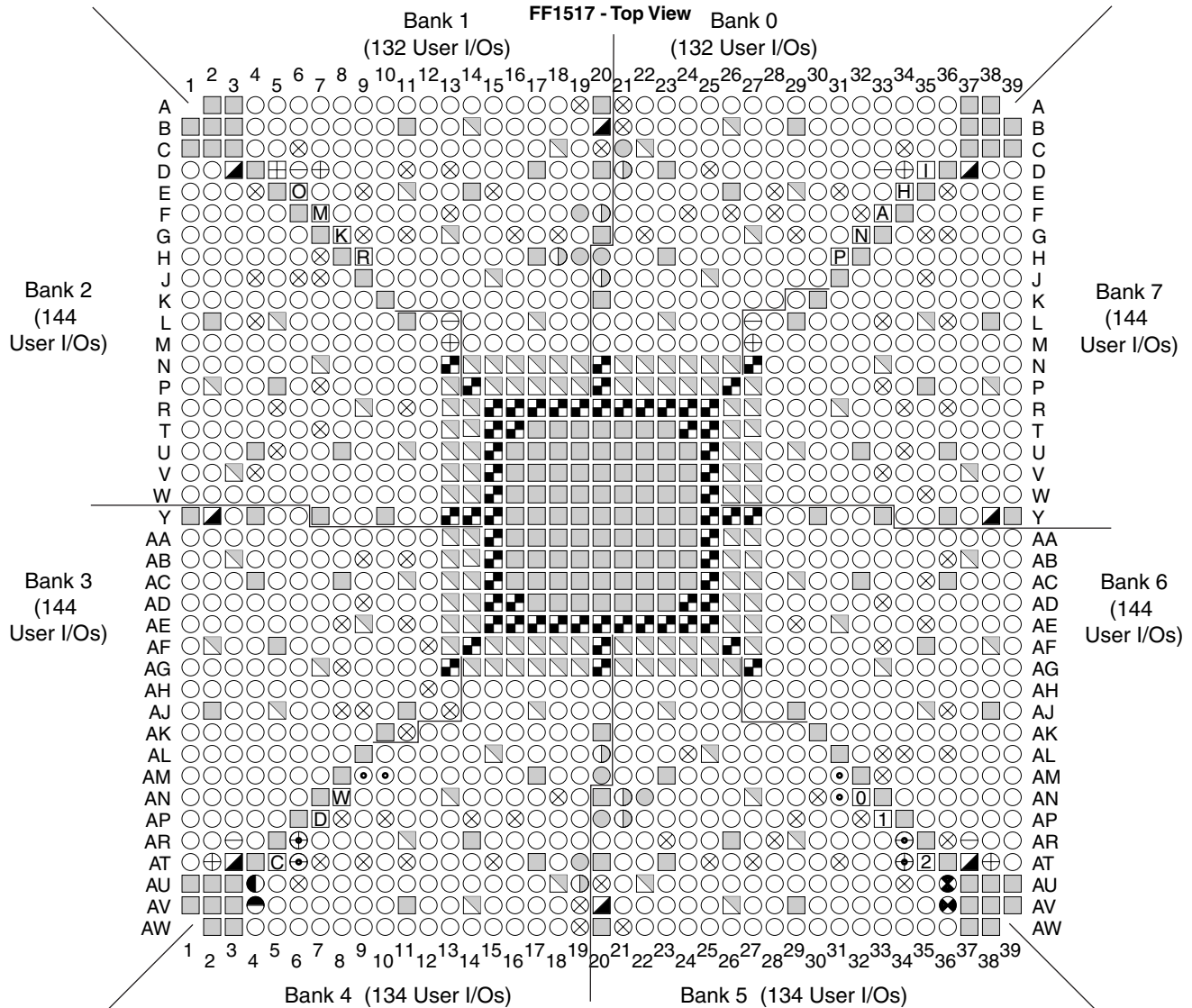
User I/O Pins	Dedicated Pins	
	<b>C</b> CCLK	<b>N</b> DXN
	<b>P</b> PROG_B	<b>A</b> DXP
	<b>D</b> DONE	<b>+</b> VBATT
	<b>2 1 0</b> M2, M1, M0	<b>R</b> RSVD
	<b>H</b> HSWAP_EN	<b>▤</b> VCCAUX
	<b>K</b> TCK	<b>■</b> VCCINT
	<b>I</b> TDI	<b>■</b> GND
	<b>O</b> TDO	<b>n</b> NO CONNECT
	<b>M</b> TMS	
	<b>W</b> PWRDWN_B	

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Figure 4-22: FF1152 Dedicated Pins



## FF1517 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram



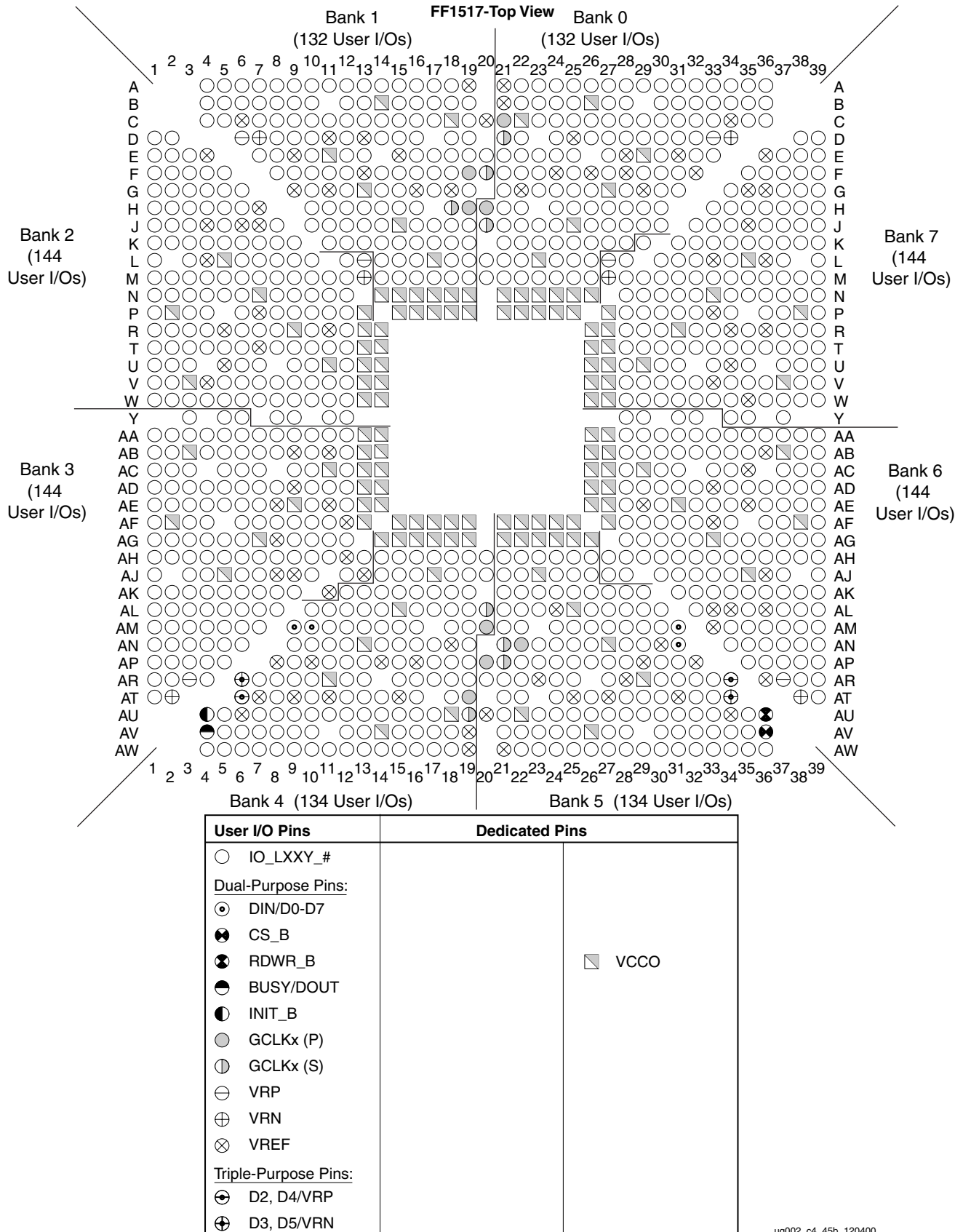
4

User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	Ⓢ CCLK	Ⓝ DXN
<u>Dual-Purpose Pins:</u>	Ⓟ PROG_B	ⓐ DXP
⊙ DIN/D0-D7	Ⓣ DONE	Ⓜ VBATT
⊗ CS_B	Ⓜ M2, M1, M0	Ⓡ RSVD
⊗ RDWR_B	Ⓜ HSWAP_EN	Ⓝ VCCO
⊗ BUSY/DOUT	Ⓚ TCK	Ⓝ VCCAUX
⊗ INIT_B	Ⓜ TDI	Ⓝ VCCINT
⊗ GCLKx (P)	Ⓚ TDO	Ⓝ GND
⊗ GCLKx (S)	Ⓜ TMS	Ⓝ NO CONNECT
⊗ VRP	Ⓜ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊕ D2, D4/VRP		
⊕ D3, D5/VRN		

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Figure 4-23: FF1517 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram

FF1517 Bank Information

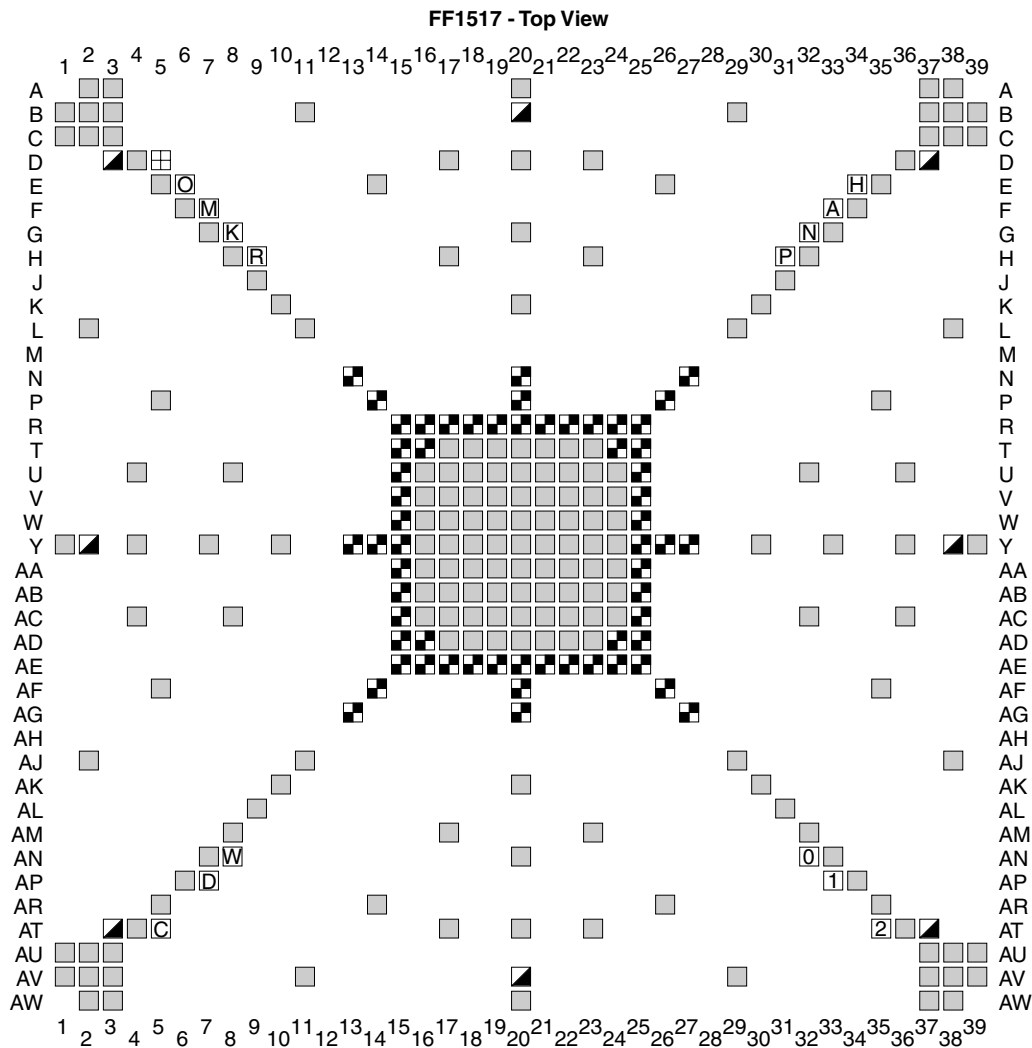


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Figure 4-24: FF1517 Bank Information



### FF1517 Dedicated Pins



4

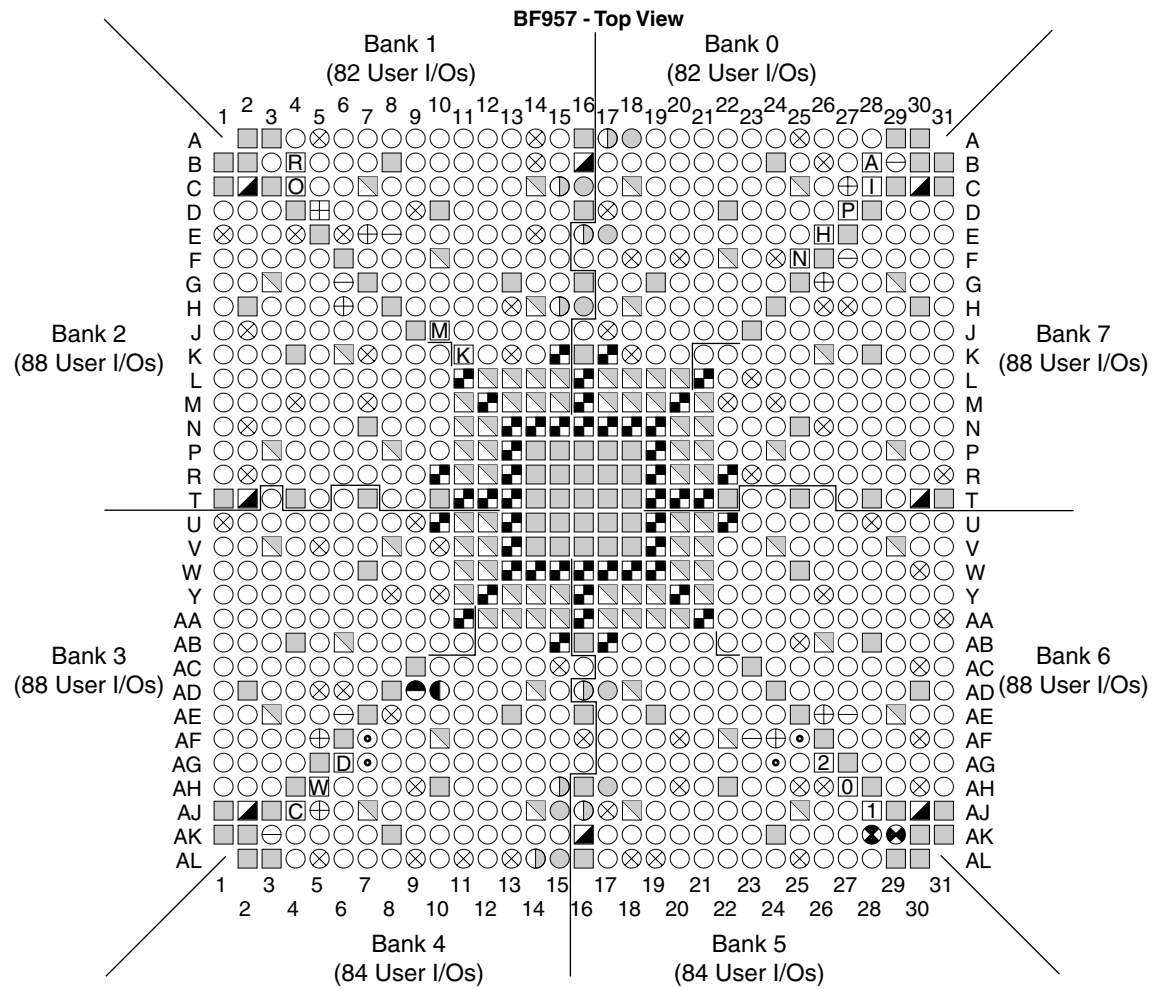
User I/O Pins	Dedicated Pins	
	<ul style="list-style-type: none"> <li>Ⓢ CCLK</li> <li>Ⓟ PROG_B</li> <li>Ⓣ DONE</li> <li>②①①① M2, M1, M0</li> <li>Ⓜ HSWAP_EN</li> <li>Ⓚ TCK</li> <li>Ⓛ TDI</li> <li>Ⓞ TDO</li> <li>Ⓜ TMS</li> <li>Ⓦ PWRDWN_B</li> </ul>	<ul style="list-style-type: none"> <li>Ⓝ DXN</li> <li>ⓐ DXP</li> <li>Ⓢ VBATT</li> <li>Ⓡ RSVD</li> <li>▣ VCCAUX</li> <li>▣ VCCINT</li> <li>■ GND</li> <li>Ⓝ NO CONNECT</li> </ul>

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Figure 4-25: FF1517 Dedicated Pins



## BF957 Flip-Chip BGA Composite Pinout Diagram



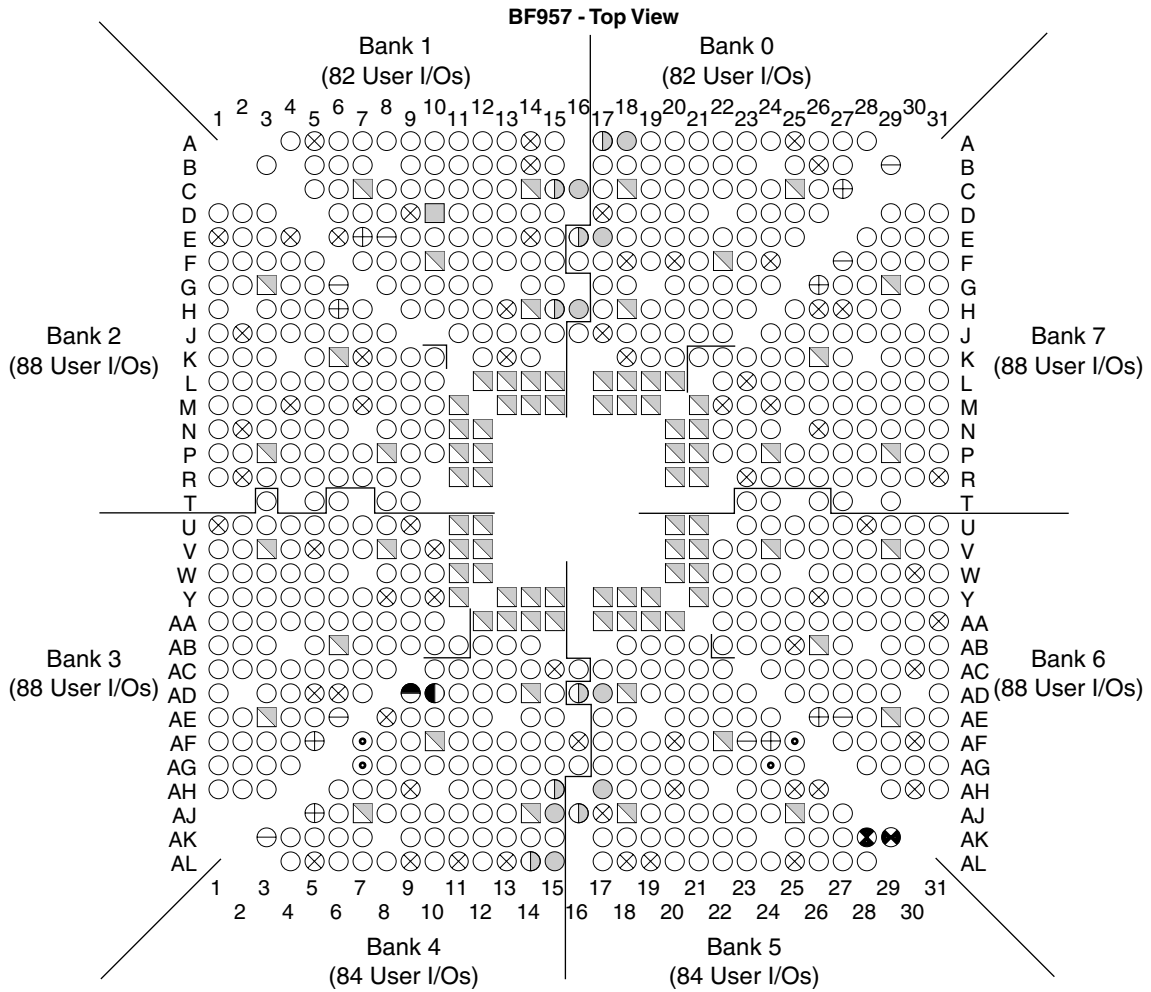
4

User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	Ⓒ CCLK	Ⓐ DXP
<u>Dual-Purpose Pins:</u>	⒫ PROG_B	⊞ VBATT
⊙ DIN/D0-D7	Ⓓ DONE	Ⓕ RSVD
⊗ CS_B	Ⓜ M2, M1, M0	⊞ VCCO
⊗ RDWR_B	Ⓗ HSWAP_EN	⬛ VCCAUX
⊖ BUSY/DOUT	Ⓘ TCK	⬛ VCCINT
⬤ INIT_B	Ⓛ TDI	⬜ GND
⊙ GCLKx (P)	Ⓞ TDO	Ⓜ NO CONNECT
⊙ GCLKx (S)	Ⓜ TMS	
⊖ VRP	Ⓜ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊖⊕ D2, D4/VRP		
⊕⊗ D3, D5/VRN		

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Figure 4-26: BF957 Flip-Chip BGA Composite Pinout Diagram

BF957 Bank Information

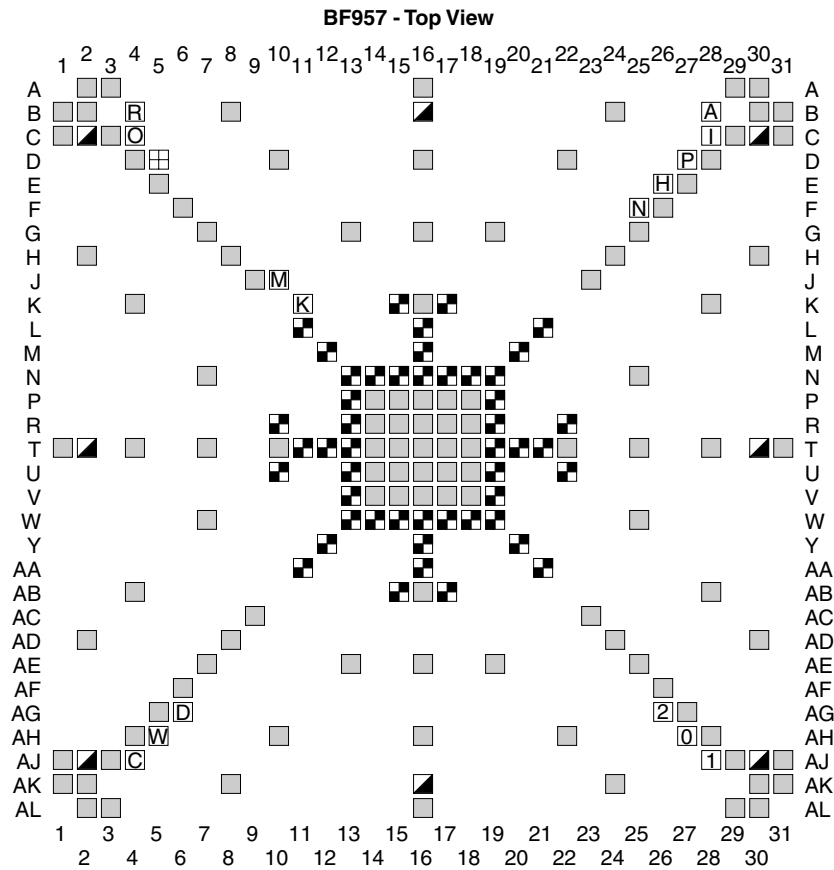


User I/O Pins	Dedicated Pins	
○ IO_LXXY_#		
<u>Dual-Purpose Pins:</u>		
⊙ DIN/D0-D7		
⊗ CS_B		
⊗ RDWR_B		▣ VCCO
● BUSY/DOUT		
◐ INIT_B		
○ GCLKx (P)		
◐ GCLKx (S)		
⊖ VRP		
⊕ VRN		
⊗ VREF		
<u>Triple-Purpose Pins:</u>		
⊖⊕ D2, D4/VRP		
⊕⊗ D3, D5/VRN		

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Figure 4-27: BF957 Bank Information

BF957 Dedicated Pins



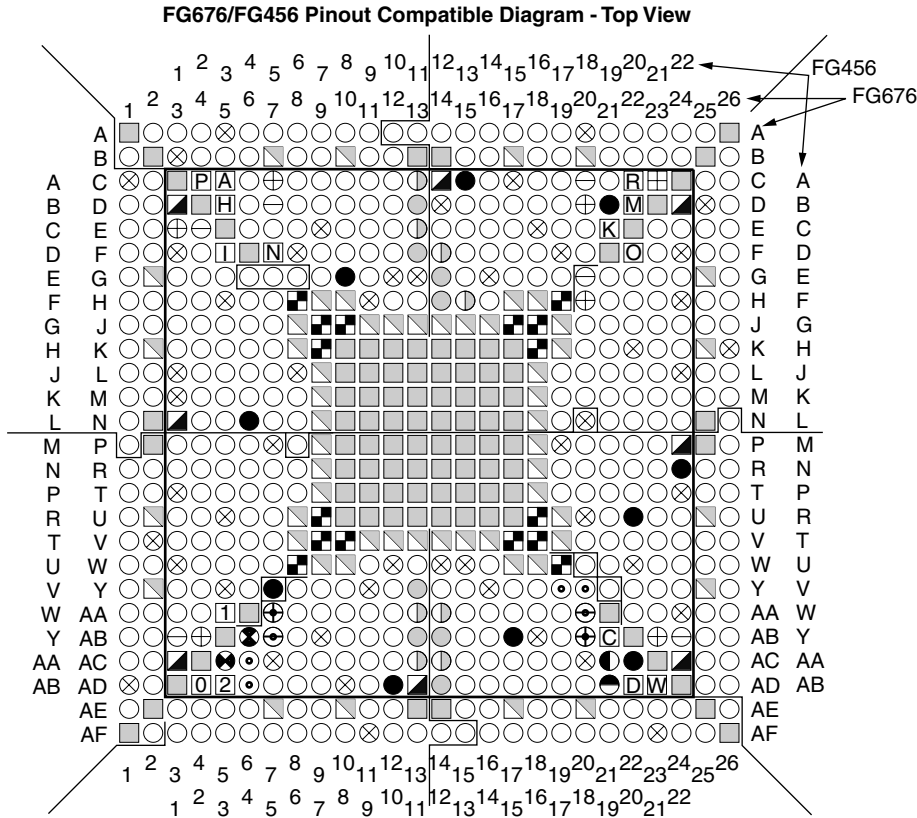
4

User I/O Pins	Dedicated Pins	
	CCLK	DXN
	PROG_B	DXP
	DONE	VBATT
	M2, M1, M0	RSVD
	HSWAP_EN	VCCAUX
	TCK	VCCINT
	TDI	GND
	TDO	NO CONNECT
	TMS	
	PWRDWN_B	

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Figure 4-28: BF957 Dedicated Pins

# FG456 - FG676 Pinout Compatibility Diagram



**Note:** FF456 is pinout compatible with FG676 with the exception of LVDS pairs and I/O  $V_{REF}$  pins in FG676 which are user I/O on FG456. In addition, some user I/O pins are not in the same bank (see  $\square$  lines)

User I/O Pins	Dedicated Pins	
$\circ$ IO_LXXY_#	$\square$ CCLK	$\square$ DXN
<b>Dual-Purpose Pins:</b>	$\square$ PROG_B	$\square$ DXP
$\odot$ DIN/D0-D7	$\square$ DONE	$\square$ VBATT
$\otimes$ CS_B	$\square$ M2, M1, M0	$\square$ RSVD
$\otimes$ RDWR_B	$\square$ HSWAP_EN	$\square$ VCCO
$\ominus$ BUSY/DOUT	$\square$ TCK	$\square$ VCCAUX
$\ominus$ INIT_B	$\square$ TDI	$\square$ VCCINT
$\ominus$ GCLKx (P)	$\square$ TDO	$\square$ GND
$\ominus$ GCLKx (S)	$\square$ TMS	$\square$ NO CONNECT
$\ominus$ VRP	$\square$ PWRDWN_B	
$\oplus$ VRN		
$\otimes$ VREF		
$\bullet$ VREF on FG676 User I/O on FG456		
<b>Triple-Purpose Pins:</b>		
$\oplus$ D2, D4/VRP		
$\oplus$ D3, D5/VRN		

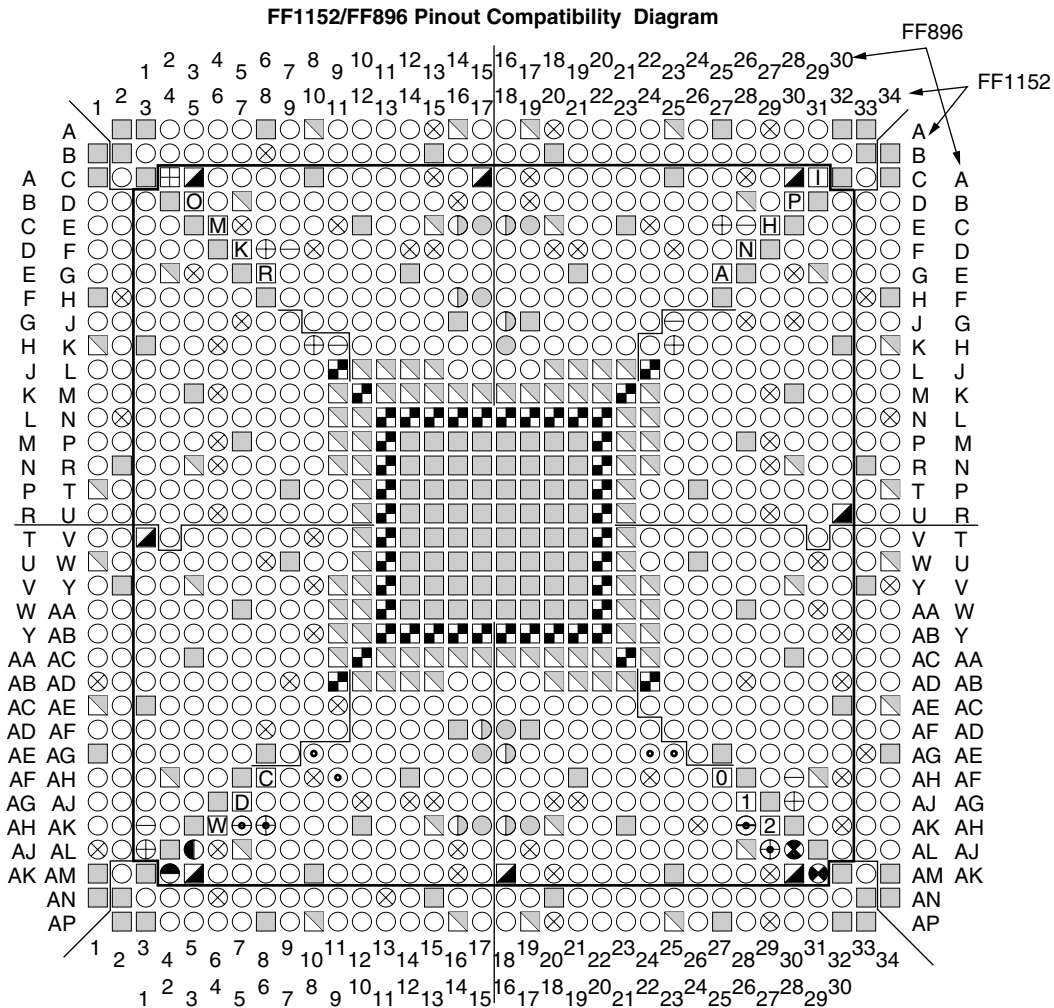
### Corresponding Pinouts

FG456	FG676
A1	C3
.	.
.	.
.	.
.	.
AB22	AD24

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Figure 4-29: FG456 - FG676 Pinout Compatibility Diagram

## FF896 - FF1152 Pinout Compatibility Diagram



Note: FF896 is 100% pinout compatible with the FF1152 except for LVDS pairs.

User I/O Pins	Dedicated Pins	
○ IO_LXXY_#	ⓐ CCLK	Ⓝ DXN
<b>Dual-Purpose Pins:</b>	ⓑ PROG_B	ⓐ DXP
⊙ DIN/D0-D7	ⓓ DONE	Ⓜ VBATT
⊗ CS_B	Ⓜ M2, M1, M0	ⓓ RSVD
⊗ RDWR_B	ⓗ HSWAP_EN	Ⓢ VCCO
⊗ BUSY/DOUT	Ⓚ TCK	Ⓢ VCCAUX
⊙ INIT_B	Ⓛ TDI	Ⓢ VCCINT
⊙ GCLKx (P)	Ⓞ TDO	Ⓢ GND
⊙ GCLKx (S)	Ⓜ TMS	Ⓢ NO CONNECT
⊖ VRP	Ⓦ PWRDWN_B	
⊕ VRN		
⊗ VREF		
<b>Triple-Purpose Pins:</b>		
⊕ D2, D4/VRP		
⊕ D3, D5/VRN		

### Corresponding Pinouts

FF896	FF1152
A2	C4
.	.
.	.
.	.
.	.
AK29	AM31

Figure 4-30: FF896 - FF1152 Pinout Compatibility Diagram

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