

# *Introduction to the Virtex-II FPGA Family*

## **Virtex-II Platform**

The Virtex-II Platform FPGA solution is the result of the largest silicon and software R&D effort in the history of programmable logic, with the goal of revolutionizing the design of complex single-chip sub-systems in terms of engineering productivity, silicon efficiency, and system flexibility.

The Virtex-II product family provides IP-Immersion™ technology which incorporates an abundance of on-chip memory options and advanced routing resources for supporting complex designs that use IP (intellectual property), such as on-chip hard-macro building blocks and a rapidly growing library of soft-IP blocks. For the first time in the programmable logic industry, innovative Virtex-II features enable system designers to:

- Eliminate external termination resistors with on-chip precision-controlled output impedance
- Manage 16 pre-engineered low-skew clock domains, with on-chip frequency and phase control
- Reduce EMI noise emissions with built-in spread spectrum clocking
- Protect chip designs with bit-stream encryption

These unique capabilities increase engineering productivity and time-to-production by supply pre-engineered solutions for signal integrity and RF noise challenges, as well as providing a secure means to deliver designs rapidly to production.

The Virtex-II Platform FPGA family is a complete programmable solution that allows digital system designers to rapidly implement a single-chip solution with density up to 10 million system gates, in weeks rather than months or years. The inherent flexibility of Xilinx FPGA devices allows unlimited design changes throughout the development and production phases of the system, with important benefits in improved productivity, reduced design risk, and higher system flexibility. This further accelerates the industry -- from custom ASICs to FPGAs -- in fields such as optical networking systems, gigabit routers, wireless cellular base stations, modem arrays, and professional video broadcast systems.

## **Virtex-II Target Applications**

The Virtex-II solution is developed specifically to enable rapid development of two of the most technically challenging digital system applications: data communications and digital signal processing (DSP) systems. High logic integration, fast and complex routing of wide busses, and extensive pipeline and FIFO memory requirements characterize these systems.

The Virtex-II family incorporates high logic capacity, up to 10 million system gates, a new Active Interconnect™ architecture optimized for predictable routing delays, an advanced memory array architecture with up to 4.5Mbits of on-chip memory, and built-in support for high-speed I/O standards at up to 1108 user pins.

Applications incorporating DSP functionality, such as echo cancellation, forward error-correction, and image compression/decompression, benefit from the abundance of embedded high-speed 18-bit x 18-bit multiplier blocks within the Virtex-II solution.

The unique features of the revolutionary Virtex-II architecture make it ideal for optical networking products, storage area networks (SANs), Voice-over-Internet-Protocol (VoIP), video broadcasting, medical imaging, wireless base-stations, and Internet infrastructure products, as well as many other products.

## Interconnect Engine for Fast, Wide Busses in Networking Applications

The Virtex-II architecture incorporates a number of novel features specifically to support wide data widths in complex networking and transmission systems. Modern complex systems operate with multiple clock domains, with large IP-based subsystems operating independently. Large, wide FIFOs and buffer memories are needed for handling fast and wide inter-subsystem data transfer. These wide busses are required both internally for intra-chip communications and externally for switched fabric communications.

For example, wide 32-bit and larger data busses can drive multiple Ultra Low-Voltage Differential Signal (ULVDS) high-speed interface standards for data transfer across a backplane or for point-to-point communications, or be used for implementing high-speed multi-cast bus standards.

These requirements challenge and exceed the capabilities of current programmable logic devices, which lack the gate capacity, memory and routing resources, performance, and architecture flexibility to fully support these designs. The Virtex-II solution is the first platform FPGA specifically targeted to improve the “ease of speed” in the development and production of these complex systems.

## Complete Solution For Rapid Time-to-Production

The Virtex-II solution combines the most flexible FPGA architecture, advanced process technology, powerful software synthesis technology, and robust IP library, to provide the most complete system integration solution today. In addition, the Virtex-II solution provides powerful features, such as XCITE™ technology, digital clock manager to help designers further reduce overall system cost and design development cycle, making Virtex-II the ideal solution for tomorrow’s high-performance system designs.