XILINX®

Bus-Structured Serial Input/Output Device

Summary

Simple shift registers are used to illustrate how 3-state busses may be used within an LCA device. Dedicated wide decoders are used to decode an I/O address range and enable the internal registers.

Specifications

Bus Width	16 Bits
Maximum Bus Speed	40 MHz
Number of Serial Channels	12
Maximum Serial Speed	60 MHz
Number of CLBs	96

Xilinx Family

XC4000

Demonstrates

3-state Buffers
Wide Decoders

Introduction

The combination of long data lines and 3-state buffers, found in Xilinx devices, is ideal for bus-structured applications. In this simple example, multiple shift registers are implemented to provide a serial input and output facility. This is purely illustrative, and the shift registers may easily be replaced with more complex functions.

In an XC4000-series LCA device, there are two horizontal Longlines equipped with 3-state buffers (T-BUFs) between each row of CLBs. In an XC4005 that has 14 rows of CLBs, there are 28 such lines. However, each of these may be split into two independent halves. This provides for construction of up-to-56-bit busses, although the number of potential bus connections is reduced.

For the purposes of this example, shown in Figure 1, a 16-bit bus is created. The flip-flops in the CLBs are used to implement the shift registers, with two bits per CLB (eight CLBs per shift register), as shown in Figure 2. The function generators preceding the flip-flops are used to select data. For loading, data is taken from the bus; for
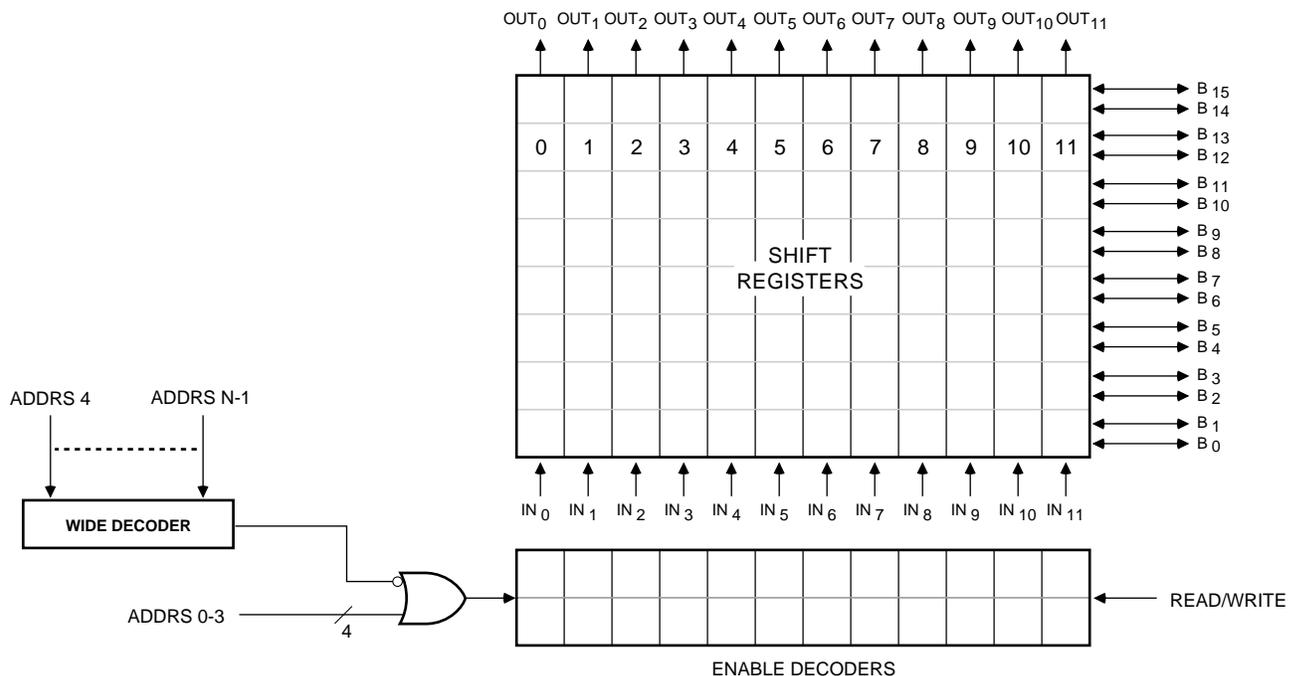

Figure 1. Serial Input/Output System

SHIFT
OUT

BUS $_{i+1}$

D   Q

D   Q

CE

BUS $_i$

LOAD/ REG   SHIFT   REG
SHIFT   IN   IN   OUTPUT
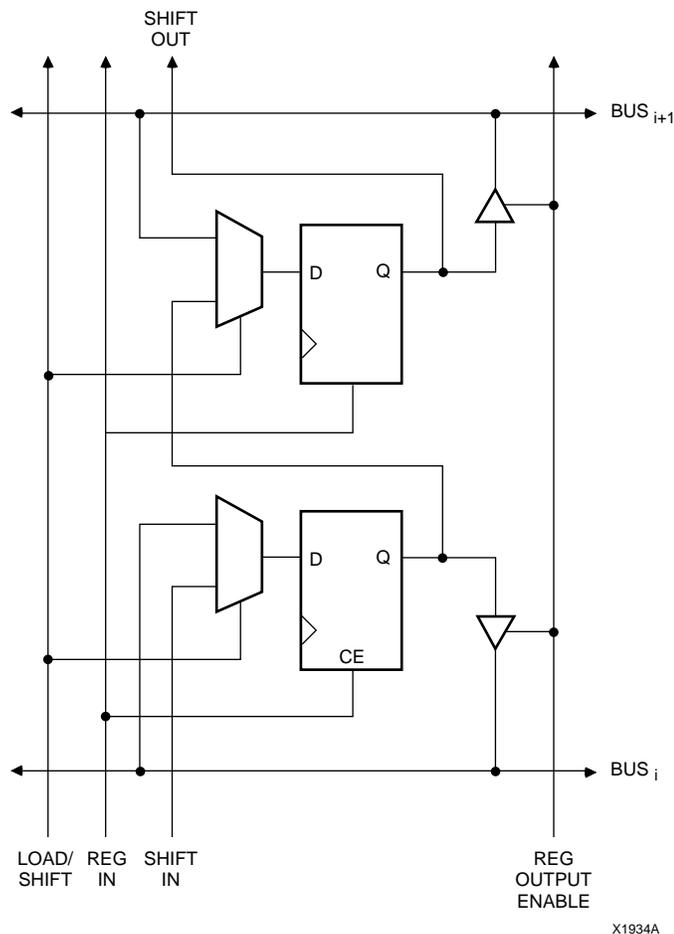   ENABLE

X1934A

Figure 2. Shift Register CLB

select data. For loading, data is taken from the bus; for shifting, it is taken from the adjacent flip-flop. A register enable is also provided, that must be asserted for either loading or shifting the register.

The connections to the bus are also shown in this diagram. A bidirectional bus has been chosen; both the inputs and outputs are connected to it. Alternatively, separate input and output busses could have been used. One Longline would broadcast data to the shift registers, and a second Longline would use the T-BUFs to multiplex the parallel outputs of the shift register. These busses could remain separate through the chip interface, or be combined into a single, bidirectional bus in the IOBs. Similarly, the shift-register inputs and outputs could remain separated, or combined for bidirectional operation.

Allowing space for control logic, 12 shift registers may be comfortably fitted onto the bus. These require a 4-bit bus address. This can be routed across the top of the shift registers and decoded at each column. A single CLB can decode the address, and use it to gate an enable signal. Two decoders are required for each shift register; one each for load enable and 3-state enable.

If these registers are part of a larger I/O register space, higher order address bits must also be decoded as chip select. Dedicated logic is provided along the edges of the chip to serve this exact purpose. Using these decoders is much faster than using CLBs, and they are free, because no CLBs are used.

In the decoder, the address bits from the IOBs are input to a wired AND. The inputs to this wired AND can be configured to be inverting or non-inverting. In this way, any fixed combination of ones and zeros can be detected. The XC4005 allows up to 28 address bits to be decoded in a single address decoder, and there are 16 such decoders.

While this totally synchronous I/O system is somewhat unrealistic, it does illustrate the use of the horizontal Longlines for bussing. If required, each shift register could have been clocked separately. This would necessitate the synchronization of the load enables to the individual clocks. However, only 120 of the 196 CLBs have been utilized, and ample space remains for this minor task and any other control functions.

While any combination of functions could be implemented and bussed together in this way, counters are particularly interesting. The dedicated carry logic embedded into each CLB allows loadable counters to be implemented with the same density as the shift registers; two bits per CLB. This would permit the construction of a 12-channel, 16-bit counter/timer.

Note: Implementing the extensive bus structure discussed in this Application Note requires considerable expertise in LCA design. The designer must specify the Longlines to be used, and constrain the placement of logic around them. The approach is only recommended for experienced LCA designers.