I/O Characteristics of the 'XL FPGAs

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Application Note by PETER ALFKE and BOB CONN

Summary

Data sheets describe I/O parameters in digital terms, providing tested and guaranteed worst-case values. This application note describes I/O parameters in analog terms, giving the designer a better understanding of the circuit behavior. Such parameters are, however, not production-tested and are, therefore, not guaranteed.

Xilinx Families

XC4000XL, XC4000XV, and Spartan-XL

Inputs

Input threshold, the voltage where a 0 changes to a 1 and vice versa, is stable over temperature, but proportional to V_{CC}:

37 to 38% of V_{CC} for the falling threshold, 39 to 42% for the rising threshold. There is 50 mV to 150 mV of hysteresis, smallest at hot and high V_{CC}, largest at cold and low V_{CC}.

5-V Tolerant Inputs

Currently, many systems use a mixture of older 5-V devices and newer 3.3-V devices. This can pose a problem when a 5-V logic High drives a 3.3-V input. See Figure 1.

On most CMOS ICs each signal pin has a clamp diode to V_{CC}, to protect the circuit against electrostatic discharge (ESD). This diode starts conducting when the pin is driven more than 0.7 V positive with respect to its V_{CC}. In mixed-voltage systems, this diode presents a problem since it might conduct tens of milliamps whenever a 5-V logic High is connected to a 3.3 V input.

In the XC4000XL/XV and SpartanXL devices, Xilinx has overcome this difficulty by eliminating the clamp diode between the device pins and V_{CC}. The pins can thus be driven as High as 5.5 V, irrespective of the actual supplyvoltage on the receiving input. These devices are, therefore, unconditionally 5-V tolerant, and the user can ignore all interface precautions, and need not worry about power sequencing.

Excellent ESD protection (up to several thousand volts) is achieved by means of a patented diode-transistor structure that connects to ground, and not to V_{CC}. The structure behaves like a Zener diode; it becomes conductive at >6 V and diverts the charge or current directly to ground. It can handle current spikes of several hundred milliamps, but continuous current must be kept below 20 mA to avoid reliability problems caused by on-chip metal migration.

See also the application note "Supply-Voltage Migration, 5 V to 3.3 V", XAPP080, available at www.xilinx.com.

PCI-Compliance

The 'XL-I/O is designed to be PCI compliant and also to be 5-V tolerant.

- 3.3-V PCI compliance requires a clamping diode to V_{CC}.
- 5-V PCI compliance does not explicitly require such a diode, but requires passing the specified PCI overshoot test.
- 5-V tolerance does not permit such a diode.

To satisfy these conflicting requirements, an internal diode is added to each output, with its cathode connected to an internal V_{TT} rail. See Figure 2.

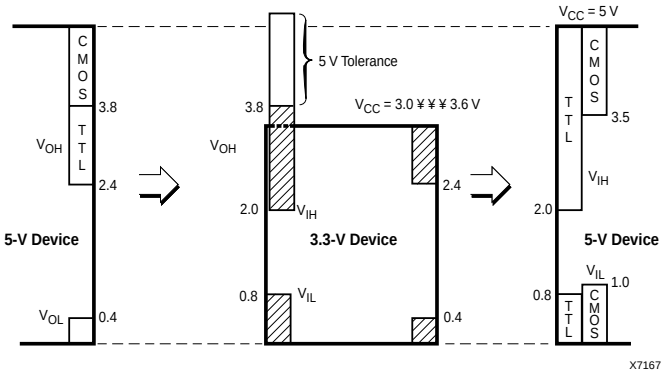

Figure 2: Interface Levels

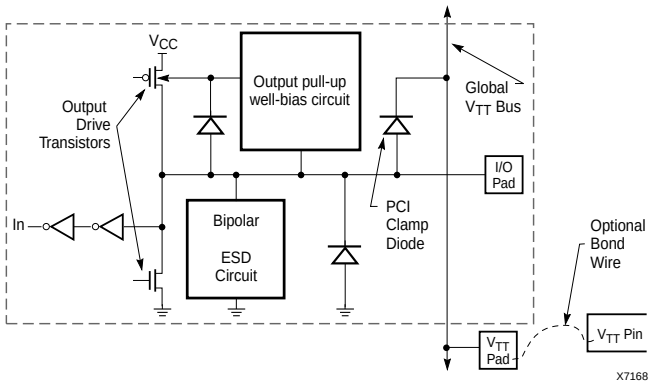

Figure 3: Simplified 'XL-I/O Structure

In the PCI-compliant XC4000XLT devices, this rail is internally bonded to eight device pins which externally must be connected to the appropriate V_{CC} supply (5 V or 3.3 V).

In all other 'XL devices, the V_{TT} rail is internally left unconnected, thus assuring 5-V tolerance.

Outputs

Sink and Source Capability

The IBIS files describe the strength of the CMOS output drivers as black boxes, giving only voltage/current values without revealing proprietary circuit details. IBIS gives an unnecessarily large set of numbers, when most users just want to know the strength of the pull-down transistor (sink capability) and the pull-up transistor (source capability). Close to either rail, the outputs are resistive, i.e. voltage is proportional to current.

Table 1 condenses the information and expresses it as output resistance in Ohm for a sink voltage less than 1 V above ground, and a source voltage less than 1 V below V_{CC}. (Data based on SPICE simulation).

Table 2: Sink and Source Capability

Device Family	Sink Resistance to GND	Source Resistance to VCC	
XC4000E	22.1 - 27.7	53.3 - 90.5	Ohm
XC4000EX	14.4 - 18.8	48.0 - 58.7	Ohm
XC4000XL/XV Spartan-XL	14.4 - 20.5	28.0 - 41.0	Ohm
Optional on all XC4000XV*	8.0 - 12.0*	20.0 - 30.0*	Ohm

* This per-pin option will also be available on all XC4000XL and Spartan-XL devices later in 1998.

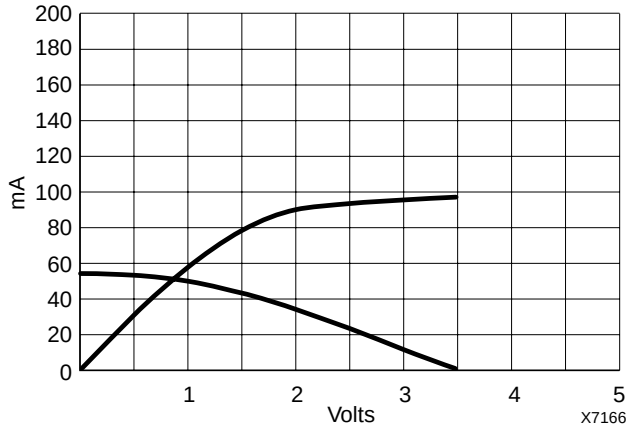

Figure 4: Output Voltage/ Current Characteristics (default for XC4000XL,

Effect of Additional Capacitive Load

Transition Time

At the specified 50 pF external load, the rise time is 2.4 ns, and the fall time is 2.0 ns. For additional capacitive loads, add 60 ps/pF to the rise time, and 40 ps/pF to the fall time.

Delay

Add 30 ps/pF to the rising-edge delay at 3.0 V.
Add 23 ps/pF to the rising-edge delay at 3.6 V.
Add 25 ps/pF to the falling-edge delay at any voltage.

The values were derived from XC4028XL measurements using the fast output option, but the slew-rate limited output option behaves almost identically.

These results are consistent with the IBIS-derived output impedance, since the delay increases with approximately one RC time constant, and the rise and fall times increase each with approximately two time constants.

These are not guaranteed and tested parameters; they are established by measuring a few devices. Xilinx, therefore, suggests that the user add a 20% guardband (multiply by 1.20) when calculating additional delay due to capacitive load above the guaranteed test limit of 50 pF.

For the same reason, subtract 20% (multiply by 0.80) when calculating the delay reduction due to a capacitive load that is less than 50 pF external. See Figure 4.

When comparing Xilinx numbers to those from other vendors who use 35 pF as a standard load, reduce the Xilinx-specified delay by 0.4 ns. Reduce the Xilinx-specified rise time by 1.0 ns and the fall time by 0.6 ns, thus changing both to 1.4 ns.

Example:

For an external lumped capacitive load of 200 pF, the rising-edge delay at 3.0 V increases by 1.2 • 150 • 30 = 5.4 ns over the guaranteed data sheet value.

The rising-edge transition time increases by an amount of 1.2 • 150 pF • 60 ps/pF = 10.8 ns over the 50-pF transition time of 2.4 ns. The rise time is thus 13.2 ns.

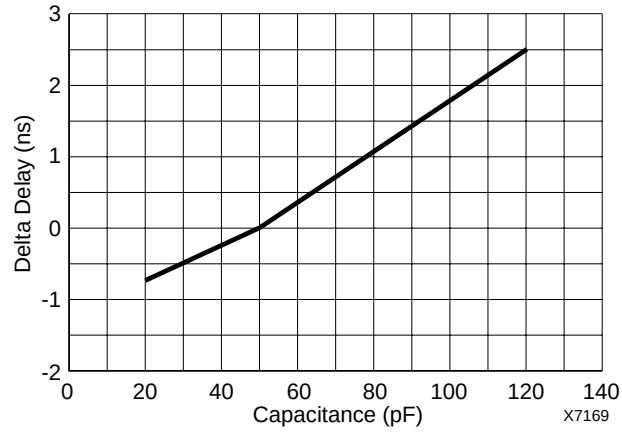

Figure 5: Additional Delay at Various Capactive Loads