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Utilizing XPLA3 Universal Control Terms

Summary

This document highlights the advantages of utilizing the universal control terms provided in the CoolRunner™ XPLA3 CPLD architecture. Design examples showing the efficiency of these universal control terms are discussed.

Introduction

The XPLA3 CoolRunner CPLD family provides unique architectural features that offer efficient design utilization within the device and great benefits to designers. One such feature is the universal control term networks. XPLA3 devices provide four universal control terms that are available to all macrocells within the device. This provides efficient utilization of common product terms that are used as clocks, output enables, resets, and presets.These control terms can be generated once and then used throughout the device. In other architectures, it may be necessary to replicate the logic generating these control terms in multiple logic blocks, thus wasting device resources.

A brief overview of the XPLA3 architecture as it pertains to the generation and networking of the local and universal control terms will be described in the following sections. This application note will also describe design instances that benefit from the use of universal control terms. The XPLA3 architecture will not be fully described in this application note, for more details on the XPLA3 architecture, please refer to white paper WP105, "XPLA3 CoolRunner CPLD Architecture Overview".

CoolRunner XPLA3 Architecture

The CoolRunner XPLA3 architecture consists of logic blocks that are interconnected by a routing matrix called the Zero-power Interconnect Array (ZIA). Each logic block contains 16 macrocells. The block diagram for a 64 macrocell device is shown in Figure 1. There are four universal control terms available to all logic blocks in a XPLA3 CPLD—a universal clock (UCLK), a universal reset (URST), a universal preset (UPST), and a universal output enable (UOE). One control term from each logic block is routed to a set of multiplexers that generates the four universal control terms. The universal control terms are then routed to each logic block for use by the macrocells.

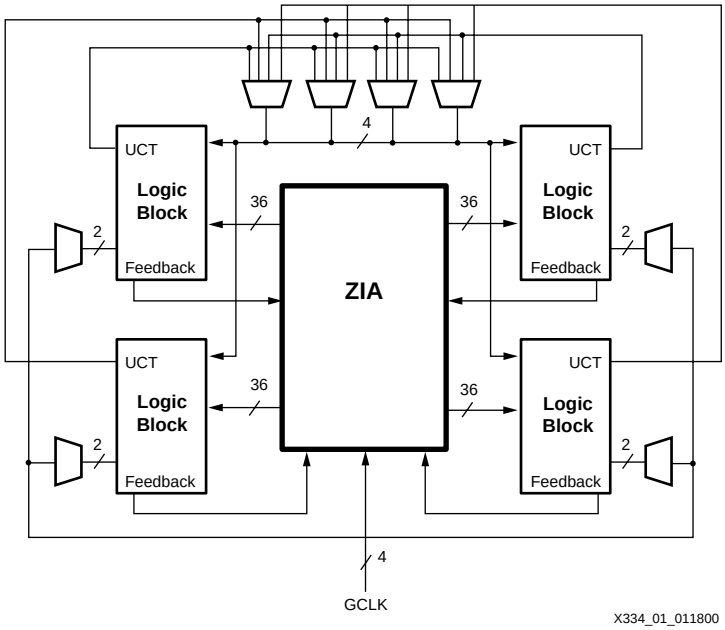

Figure 1: **XPLA3 High-level Architecture (64 Macrocell Device Shown)**

Each logic block contains a pure PLA array (programmable AND, programmable OR) as shown in Figure 2. The PLA array provides a pool of 48 product terms that can be used as macrocell clocks, to generate control terms (reset, preset, clock enables, or output enables), or as needed by the 16 macrocells in the logic block. The first eight product terms in the PLA are used to generate eight Local Control Terms (LCT[0:7]). Note that if these product terms are not needed as control terms, they are available for other logic. Local Control Term 7 (LCT7) is routed from the logic block to the universal control term multiplexers.

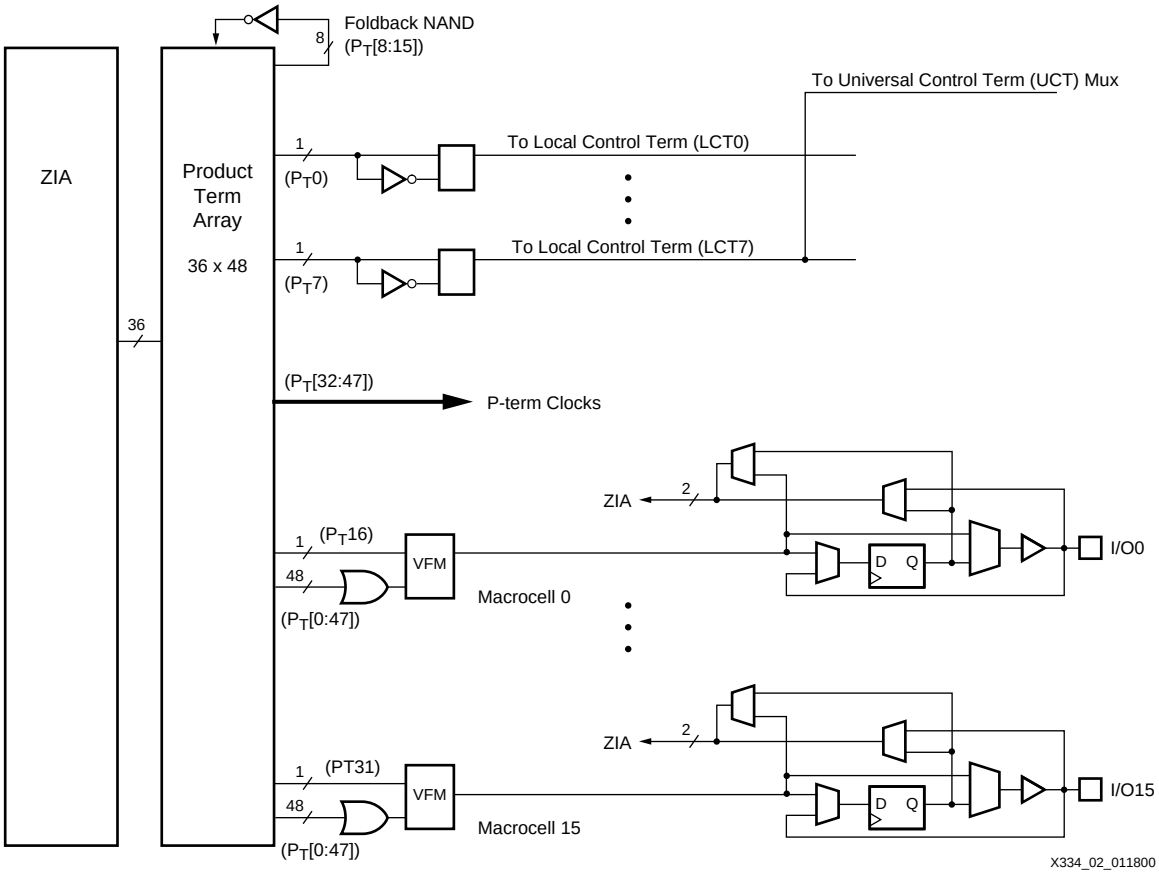

Figure 2: **XPLA3 Logic Block Architecture**

As seen in Figure 3, both local and universal control terms are used in the macrocell as the macrocell register clock, reset, and preset functions as well as the output enable for the output buffer. In addition, local control terms can be used as a hardware clock enable.

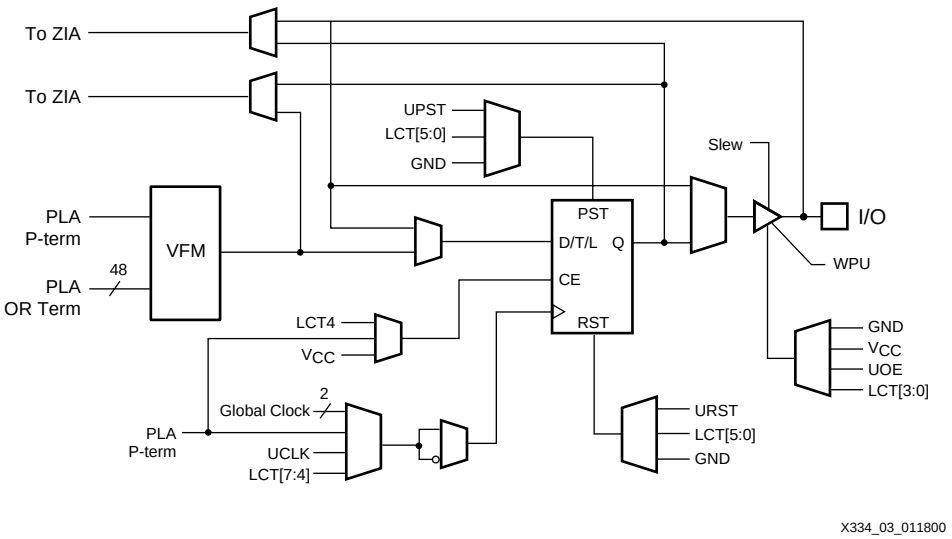

Figure 3: **XPLA3 Macrocell**

Utilizing the Universal Output Enable

Each logic block in a CoolRunner XPLA3 contains 16 macrocells, but the number of I/O per logic block varies with device size and package. Many applications require that a CPLD design interface to a 16-bit data bus or larger. Depending on the selected CPLD and package, one logic block may not contain 16 I/O connections, therefore, the data bus is implemented in multiple logic blocks.

Consider the case where a CPLD design is interfacing to a microcontroller. The data bus can be 16 bits and bidirectional, requiring that the data bus be controlled with an output enable. This output enable will generally be the result of decoding address bits and the read/write signal. Due to the fact that not all macrocells in the logic block are bonded to I/O pins, the data bus will be implemented in multiple logic blocks.

Implementing this type of design in an XPLA3 CPLD allows the logic generating the output enable signal for the data bus to be implemented once in only one logic block. The software will use LCT7 from one logic block for the Universal Output Enable (UOE) signal. This signal is then available to all logic blocks within the device and can control the bidirectional data bus where ever these bits are implemented.

Note that the presence of the UOE signal has the additional advantage of allowing great flexibility in the placement of the data bus in the device, i.e., the fitter is not restricted to placing the data bus in certain logic blocks that have access to the output enable signal. Also, the fitter can choose which logic block to implement the output enable equation—it does not even need to be a logic block containing any portion of the data bus. Device utilization is increased because the fitter does not need to replicate the logic to generate the output enable control term in multiple logic blocks. If product terms [0:7] in each logic block are not used for control term generation, they are available for other logic. Therefore, the use of the universal control term makes more product terms available for the implementation of additional logic.

Utilizing the Universal Reset and/or Preset

Many applications require the use of counters of various sizes that may need to be preset or reset based on conditions other than system reset or power-up. One example of such an application is where a counter within the CPLD is used to implement a watch-dog timer. Watch-dog timers are generally used in microcontroller type applications to insure that the system is operating properly. The microcontroller software is written so that the counter reset is generated periodically. This counter starts counting system clocks upon power-up and is reset by the microcontroller, indicating that the system software or operation is executing properly. After the reset is released, the counter again starts counting system clocks. If the counter ever reaches a terminal count (or some other pre-determined value), a system error has occurred and therefore the CPLD asserts a system reset.

In this case, the reset signal to the watchdog timer will be an input to the CPLD, but there are still advantages to using the universal reset signal (URST) to route this signal. If the URST signal is used, the counter can be placed across multiple logic blocks at the fitter's discretion. The fitter is not restricted to placing this counter in the minimum number of logic blocks due to implementing this control term in certain logic blocks. Since the URST signal is available to the entire device, the fitter can implement the reset from a control term in any logic block and the counter in multiple logic blocks throughout the device.

Note that the four universal control terms are routed independently of the ZIA, therefore implementing this reset on the URST signal does not require fan-in to the logic block from the ZIA, but allows this fan-in to be used by other signals. If the URST signal was not used, the reset signal would have to be input to each logic block through the ZIA, reducing the remaining available fan-ins that can be used by other signals. It would then require a product term in each logic block to create a local control term. This wastes product terms and does not utilize the device resources efficiently.

Though this example highlighted the advantages of the URST signal, please note that similar examples could be studied which utilize the universal preset signal (UPST).

Utilizing the Universal Clock

The XPLA3 architecture contains 4 global clock signals that must be driven from external clock sources. Many designs, however, require that an internal clock be used for large portions of the CPLD design. These designs greatly benefit from the use of the universal clock control term (UCLK).

One example of this type of application is where the CPLD implements an I^2C controller along with a microcontroller interface as shown in Figure 4. The clock provided by the microcontroller or by the system is typically much faster than that needed to drive the I^2C bus. A large portion of the CPLD design will be clocked from the system clock and the portion of the CPLD logic interfacing to the I^2C bus will be clocked by a divided version of the system clock.

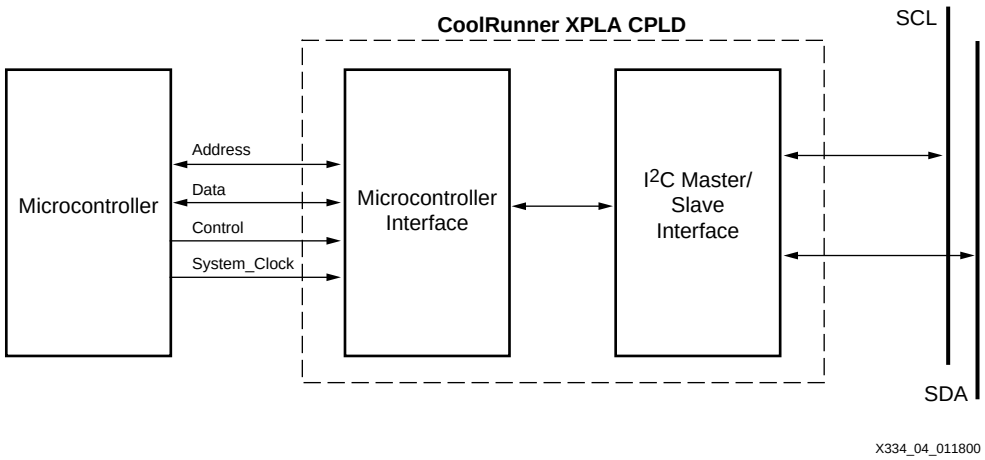

Figure 4: **CoolRunner I^2C Bus Controller**

In this case, a counter is used to divide the system clock to the 100 KHz (or 400 KHz) clock needed to drive the I^2C clock (SCL). Since an I^2C controller can both send and receive data, the I^2C portion of the CPLD logic will also need to be clocked by SCL. Therefore, the output of the counter that produces SCL will not only be output from the CPLD, but will also be routed on the universal clock signal (UCLK) to clock internal portions of the CPLD logic that interface to the I^2C bus. Routing SCL on UCLK saves local control terms, product terms, and fan-in to logic blocks.

Conclusion

The universal control terms provided in the CoolRunner XPLA3 architecture greatly increase the efficiency of resource utilization within the device. These control terms eliminate the need to replicate common logic in multiple logic blocks, reduce fan-in to the logic blocks, and reduce the number of product terms required by the design. Since the universal control terms are available to all macrocells of the device, use of these networks provides the fitter with the maximum flexibility in partitioning the logic of the design into logic blocks.

Please note that in all of the above mentioned design examples, the fitter recognizes the signals which should be routed as universal control signals and allocates the signals appropriately. The designer does not need to attach a particular property or attribute to a net to instruct the fitter to utilize these universal networks.

Revision History

Date	Version	Revision
01/31/00	1.0	Initial Xilinx release.