XILINX®

XAPP406 (v2.0) December 1, 2000

Cross Probing to Synplicity and Exemplar

Author: Yenni Totong

Summary

Xilinx Alliance software version 3.3.06i (3.1i Service Pack 6) or later has been enhanced to include logical and timing cross probing to **Synplify/Synplify Pro** and **LeonardoSpectrum**. The **logical cross probing** feature enables the user to select instances or nets in warning or error messages in the Error Viewer to cross probe back to the synthesis tool schematic view. This is useful for debugging a design with logical DRC errors/warnings. The **timing cross probing** feature enables the user to select a path, nets or instances to cross probe from the timing report within Timing Analyzer back to the synthesis tool schematic view. This feature is useful for analyzing timing problems. These functionalities can be used with **Synplify / Synplify Pro version 6.0.0 or later** from Synplicity and with **LeonardoSpectrum version 2000.1b or later** from Exemplar Logic.

Displaying the Navigation Report for Logical Cross Probing

A navigation report (NAV) file can be viewed in the new Error Viewer window now available in the Xilinx Alliance software. The NAV file is produced by the translate stage of the Flow Engine in Design Manager, or when the NGDBuild command is run from the command line. NGDBuild names the file **`<design name>_ngdbuild.nav`**. The Navigation Report icon can be found in the Design Manager Report Browser. See Figure 1.

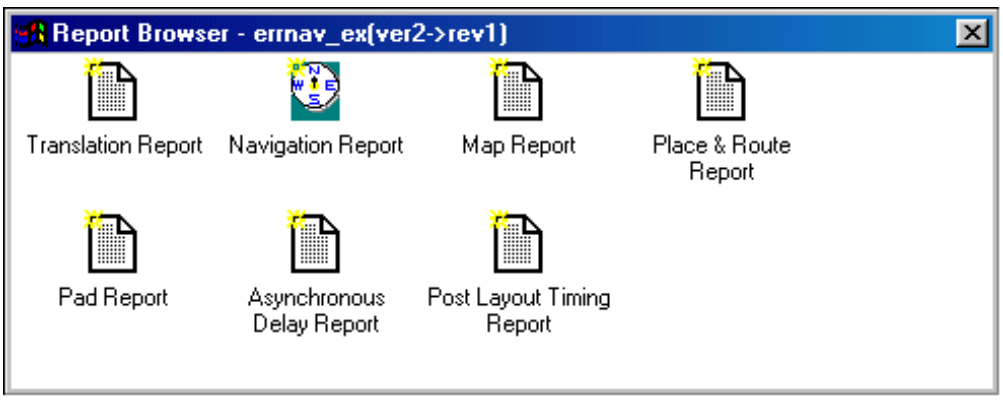


Figure 1: **Report Browser with Navigation Report Icon**

The Navigation Report icon is double clicked to launch the Error Viewer, which then displays the NAV file. The NAV file will be produced by NGDBuild even if the design produces no DRC errors or warning messages. In this case, the Error Viewer will display an empty screen.

Alternatively, the Error Viewer can be launched from the command line with the following command:

`errview` *design_name*`_ngdbuild.nav`

NOTE: The Error Viewer executable **`errview`** is located in the **`$XILINX/bin/<platform>`** directory. The **`<platform>`** can be **`hp`**, **`nt`**, or **`sol`**.

See Figure 2 for an example of a navigation report file.

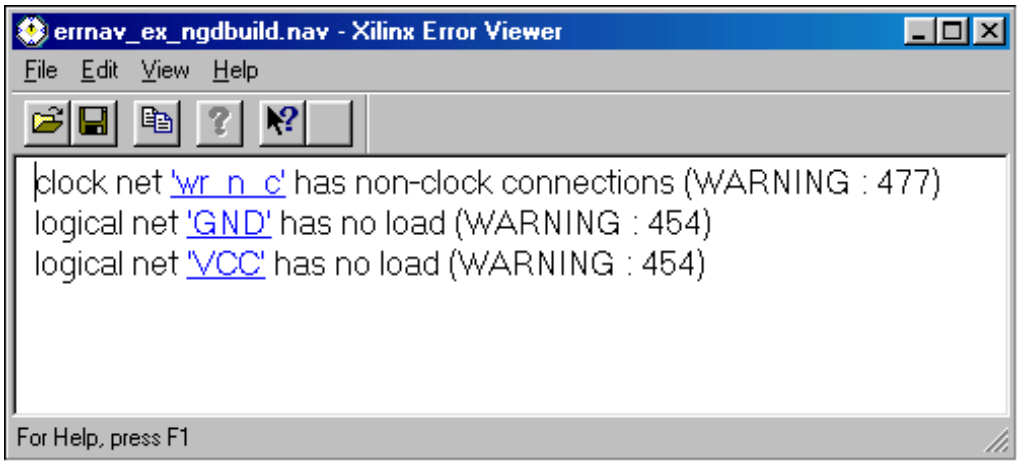


Figure 2: **Error Viewer Viewing `errnav_ex_ngdbuild.nav`**

Nets that contain warnings or errors are highlighted in blue by default. These nets are active links that can be used to navigate to the Synplify / Synplify Pro or LeonardoSpectrum schematic viewer. With the proper settings, the user can click on the highlighted net name in the Error Viewer to navigate to the corresponding net in the synthesis tool's schematic viewer.

> **Note:** The highlight color and the font in the Error Viewer can be changed from **File** → **Preference** setting.

Displaying the Navigable Timing Report for Timing Cross Probing

A **navigable timing report (XML)** file is now available in the Xilinx Alliance software.Opening the XML file in Timing Analyzer will display hyperlink of paths and instances. The paths and instances can be clicked to cross probe to Synplify/Synplify Pro or LeonardoSpectrum.

The XML file can be produced from the **"trce"** command or from the **Timing Analyzer**. The Design Manager produces an XML file by default by executing "trce" command.

Producing Navigable Timing Report (XML) File from "trce" Command

The "**trce**" command will produce an XML file if the "**-xml**" option is specified as follows:

```
trce errnav_ex.ncd errnav_ex.pcf -e 3  -o errnav_ex.twr -xml
errnav_ex_trce.xml
```

If using Design Manager, the XML file will be produced at the end of Place-and-Route stage. See Figure 3.

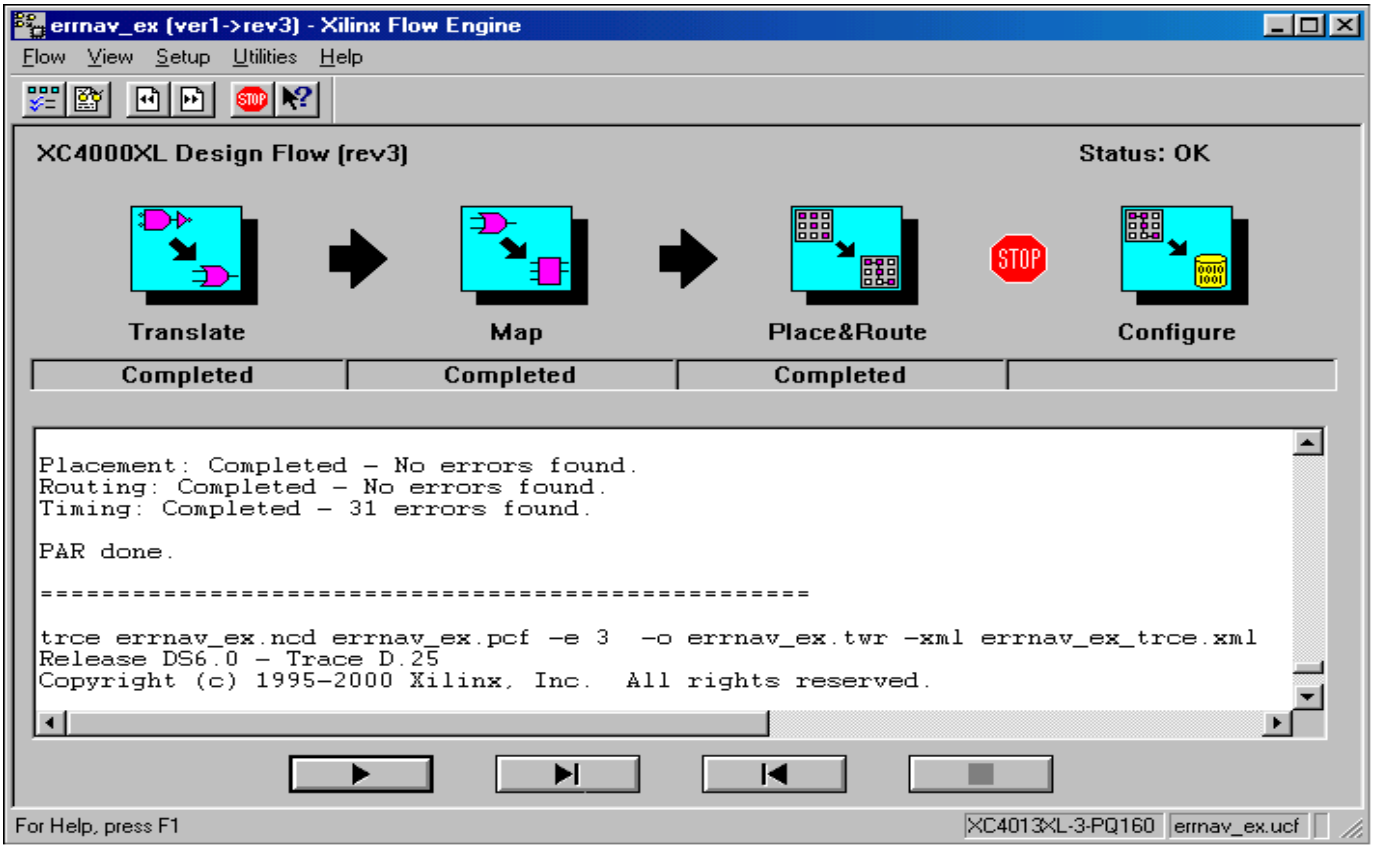


Figure 3: **Flow Engine Running "trce" to Produce XML File**

The "trce" command will be executed by Flow Engine if "Produce Post Layout Timing Report" option is checked in Design Manager. This is set by default. When the Place-and-Route stage completes, a Post Layout Timing Report with Timing Analyzer icon can be found in the Design Manager Report Browser. See Figure 4.

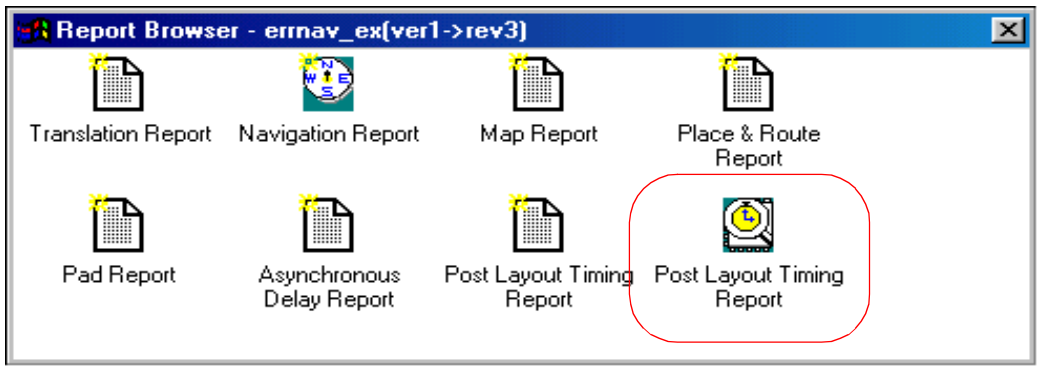


Figure 4: **Report Browser Showing Navigable Timing Report**

Double clicking the Post Layout Timing Report will open the XML file in Timing Analyzer and allows the user to do cross probing. See Figure 5.

Notes:

If there is no timing error in the design, there might not be a navigable path in the timing report.

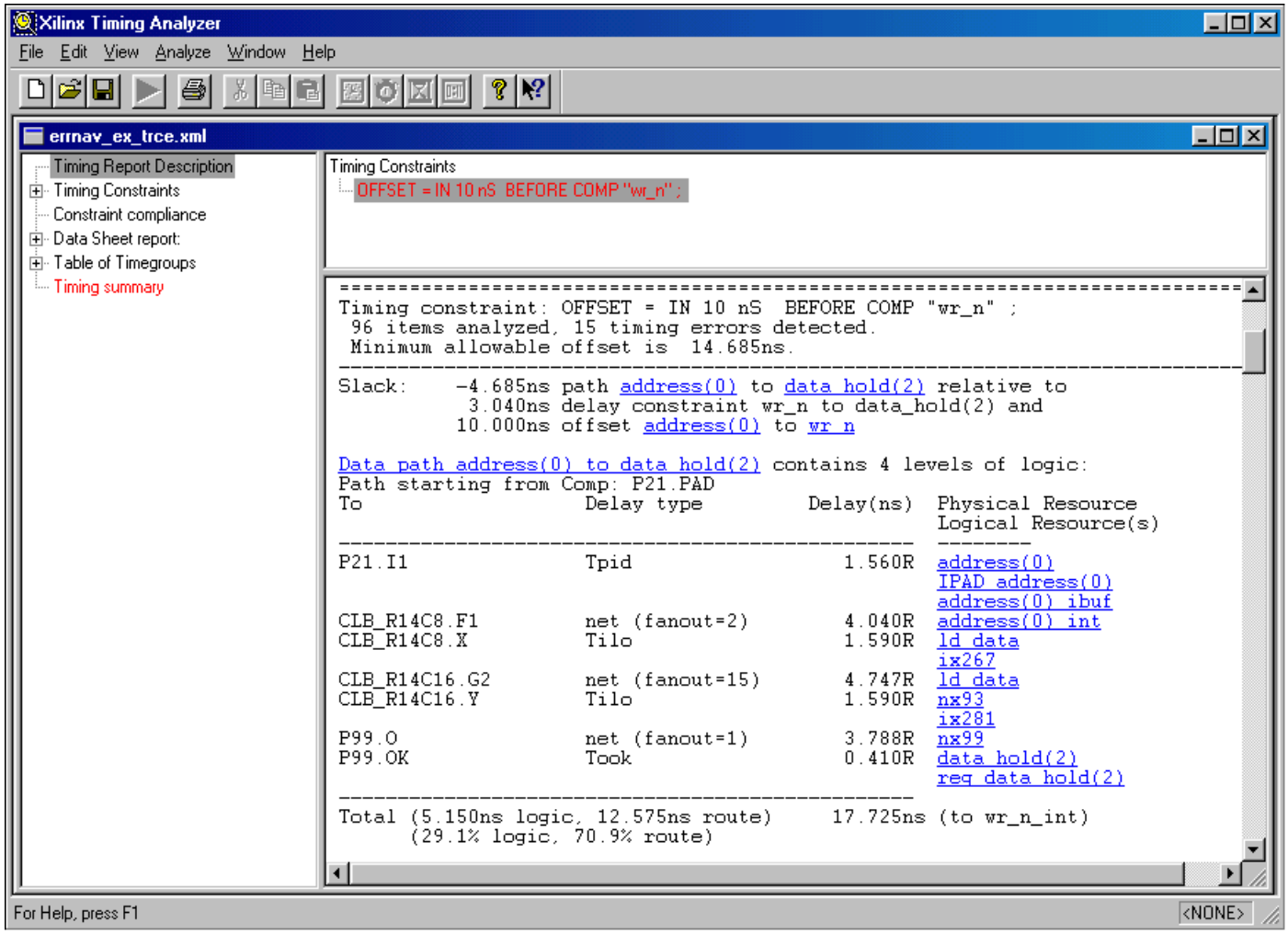


Figure 5: **XML File Displayed in Timing Analyzer**

Producing XML File from Timing Analyzer

Timing Analyzer can be executed by double-clicking its icon in Design Manager or from a command line as follows:

```
timingan <routed_design>.ncd <design>.pcf
```

When the routed NCD and the PCF files are loaded, click on **Analyze** → **Against Auto Generated Design Constraints** or other constraints to analyze. See Figure 6.

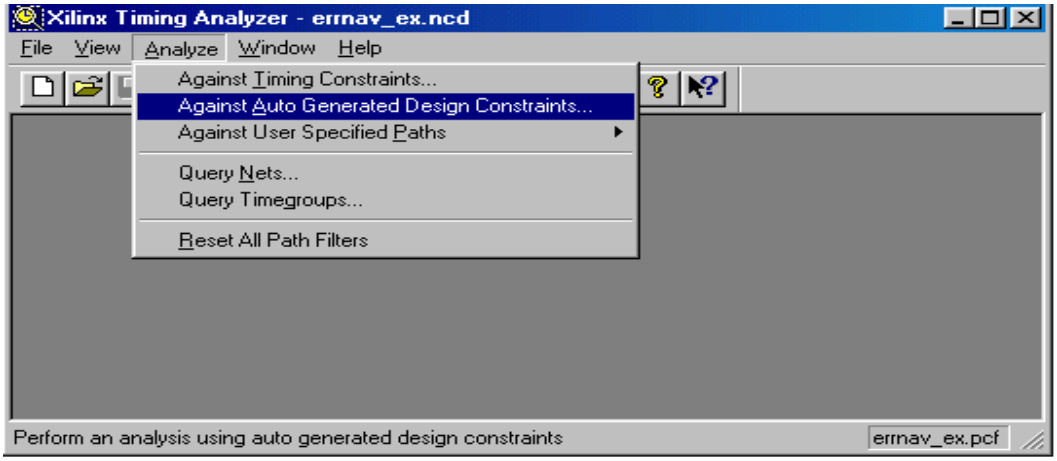


Figure 6: **Creating Timing Report from Timing Analyzer**

A timing report similar to Figure 5 will be displayed.

The timing report can be saved as .xml format for future viewing. To do this, click **File** → **Save As** and select "XML Timing Report (*_trce.xml) as the type.

Viewing a Previously Saved XML File

A previously saved XML file can be viewed in timing analyzer by typing the following command:

```
timingan <filename>_trce.xml
```

or from Timing Analyzer menu:

File → **Open** → **Timing Report**

Cross Probing with Synplify / Synplify Pro

This section describes setting up sequence, guidelines, and troubleshooting procedure for logical and timing cross probing between Xilinx and the Synplify / Synplify Pro schematic viewer.

Setup

The following describes the settings needed to do cross probing with Synplify / Synplify Pro:

1. The environment variable **`XIL_ITC_XVENDOR`** must be set to “synplicity”. There is no default value for this variable. Setting this variable to “synplicity” specifies that Synplify / Synplify Pro is the target of the cross probing applications.

   To set the environment variables, do the following:

   UNIX Platform:

   Type the following at the command line:

   ```
   setenv XIL_ITC_XVENDOR synplicity
   ```

   PC Platform:

   Set the following in the **`autoexec.bat`** or system environment setting area and reboot the PC if using Windows98.

   ```
   set XIL_ITC_XVENDOR=synplicity
   ```

1. Synthesize the design in Synplify / Synplify Pro.
2. Implement the design in the Xilinx implementation tools.

- After Translate (NGDBuild) has completed, "**Logical Cross Probing**" can be done.
- After Place-and-Route (PAR) has completed, "**Timing Cross Probing**" can be done.

Logical Cross Probing

To cross probe from the Error Viewer to Synplify, do the following:

1. Open the design project in Synplify / Synplify Pro.
2. OPTIONAL: Select **HDL Analyst** → **RTL** and select the hierarchical or flattened view.
3. Select **HDL Analyst** → **Technology** and select the hierarchical or flattened view.
4. Select **HDL Analyst** → **External Cross Probing Engaged**. This enables external cross probing.
5. Invoke the Error Viewer from Design Manager, or from the command line as described in **Displaying the Navigation Report for Logical Cross Probing**, page 1. The error viewer window will show DRC warnings and/or errors from NGDBuild with the net names highlighted as shown in Figure 7.

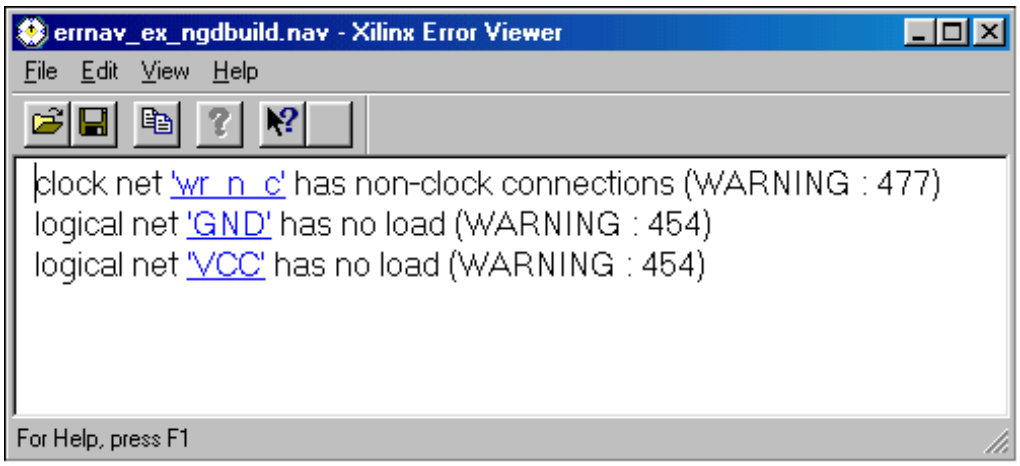


Figure 7: **Navigation Report from Synplify Synthesized Design**

6. Click on a net name in the Error Viewer window. The corresponding net should be highlighted in the Technology View window, as shown in Figure 8, page 7.

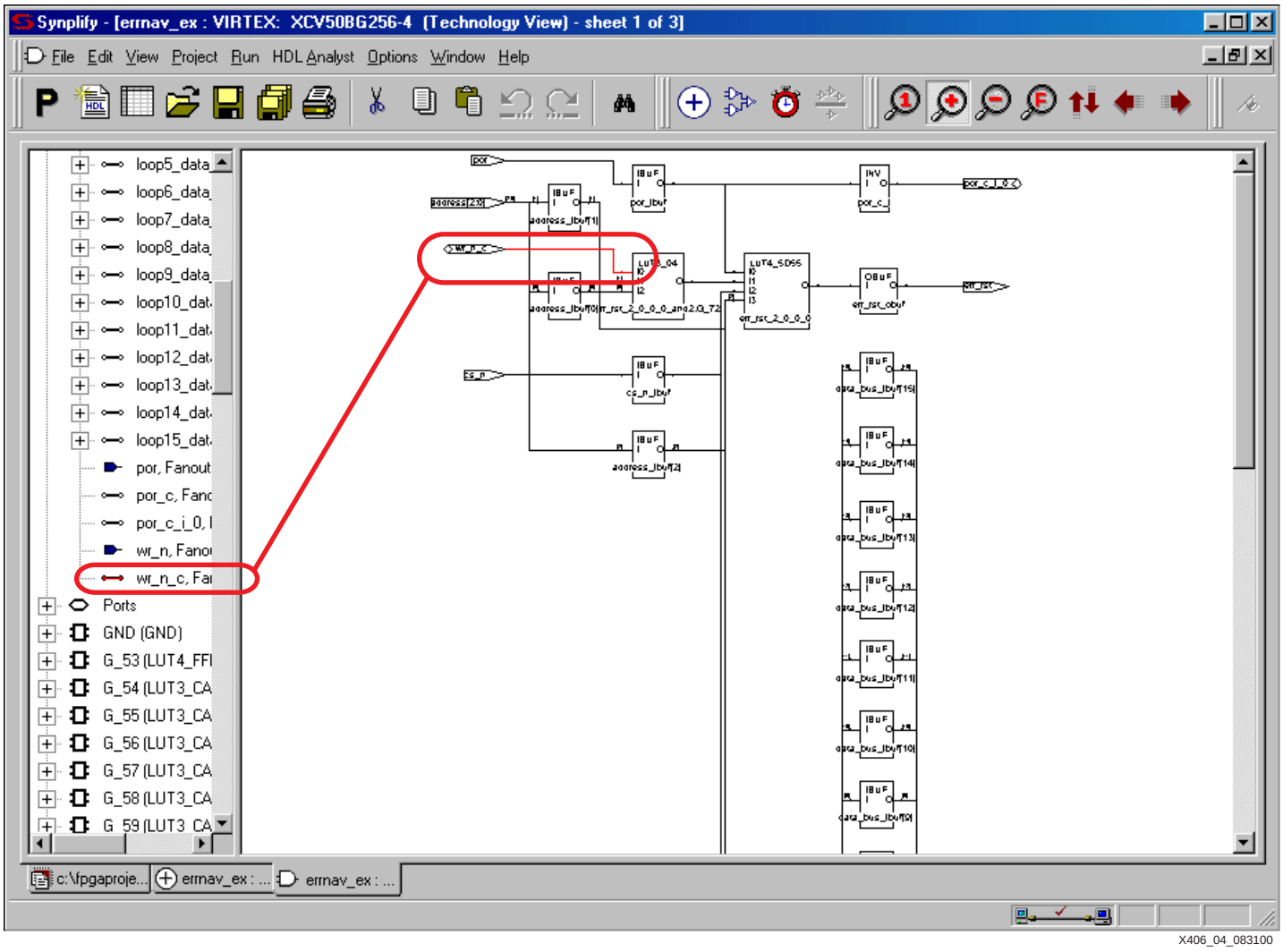


Figure 8: **Highlighted in the List and the Schematic Window: Net wr_n_c**

Timing Cross Probing

To cross probe from the Timing Report in Timing Analyzer to Synplify/Synplify Pro, do the following:

1. Open the design project in Synplify / Synplify Pro.
2. OPTIONAL: Select **HDL Analyst** → **RTL** and select the hierarchical or flattened view.
3. Select **HDL Analyst** → **Technology** and select the hierarchical or flattened view.
4. Select **HDL Analyst** → **External Cross Probing Engaged**. This enables external cross probing.
5. Display the XML file as described in **Displaying the Navigable Timing Report for Timing Cross Probing**, page 2. The timing report in the Timing Analyzer window will show navigable paths and instances as shown in Figure 9

```
Timing constraint: Default OFFSET IN BEFORE analysis for clock "wr_n_c"
 96 items analyzed, 0 timing errors detected.
 Minimum allowable offset is   9.722ns.
--------------------------------------------------------------------------------

Report:      9.722ns offset address(2) before wr_n

Data path address(2) to data_hold(9) contains 4 levels of logic:
Path starting from Comp: B2.PAD
To                    Delay type         Delay(ns)  Physical Resource
                                                    Logical Resource(s)
-------------------------------------------------  --------
B2.I                  Tiopi                0.989R  address(2)
                                                    address(2).PAD
                                                    address_ibuf[2]
CLB_R10C1.S1.G1       net (fanout=2)       3.348R  address_c(2)
CLB_R10C1.S1.Y        Tilo                 0.738R  loop15_data_hold_2(15)
                                                    G_53
CLB_R6C1.S0.F2        net (fanout=16)      2.005R  G_53
CLB_R6C1.S0.X         Tilo                 0.738R  loop9_data_hold_8(9)
                                                    G_63
M2.O                  net (fanout=1)       1.909R  loop9_data_hold_8(9)
M2.CLK                Tioock               1.292R  data_hold(9)
                                                    data_hold[9]
-------------------------------------------------
Total (3.757ns logic, 7.262ns route)      11.019ns (to wr_n_c)
      (34.1% logic, 65.9% route)
```

Figure 9: **Path Selected to Cross Probe to Synplify Schematic Window**

6. Click on any path or instance once to enable cross probing for Timing Analyzer.
7. Click on the path or instance to cross probe. The corresponding path or instance should be highlighted in the Technology View window, as shown in Figure 10.

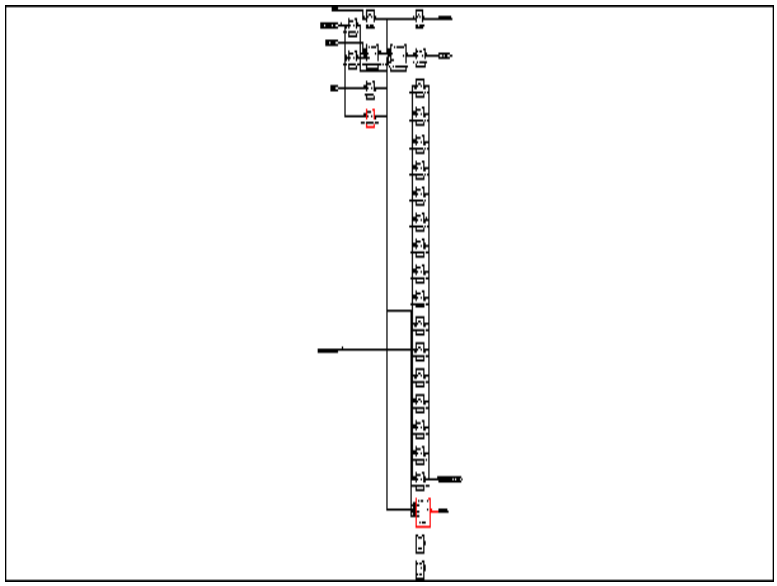


Figure 10: **Selected Path Highlighted in Synplify Technology View**

8. To isolate the schematic to show only the selected path, right click on the Technology View window and select **Filter Schematic**. The filtered path is shown in Figure 11.

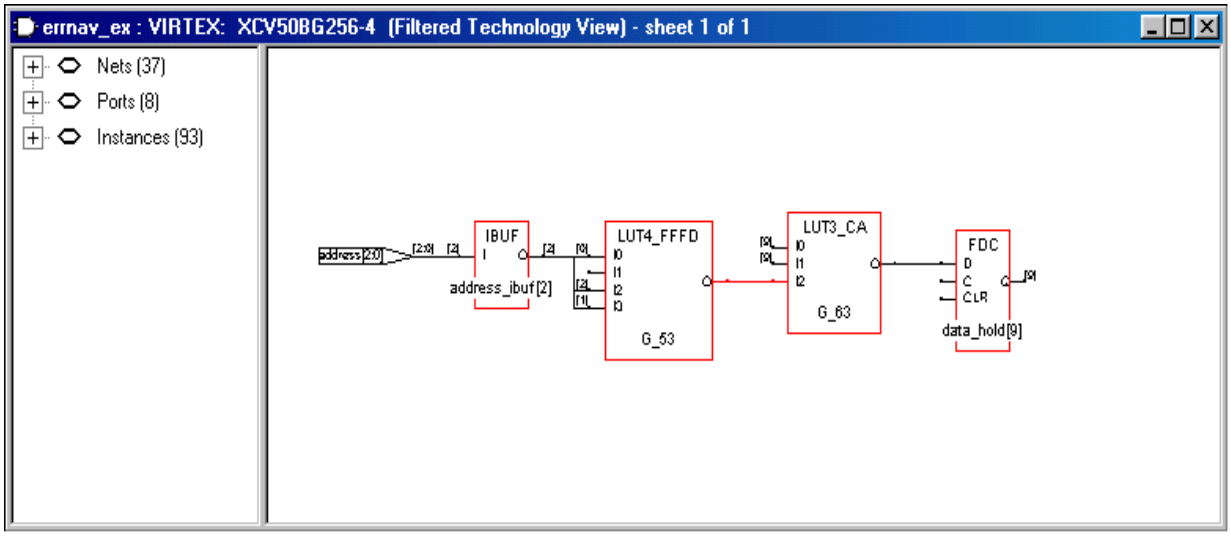


Figure 11: **Filtered Path in Synplify Technology View**

Locating Nets and Instances in the Schematic View

The following are guidelines on how to locate a net/path/instance in Synplify/Synplify PRO:

1. Most instances/nets/paths can cross probe only to the Technology View.

   In Synplify/Synplify Pro, net and instance names are altered in synthesis during technology mapping. This causes the names in the RTL View to differ from the names in the Technology View. On the other hand, Xilinx's Implementation tools get the net/instance names from the EDIF netlist which are identical to the names in the Technology View. Since the logical and timing cross probing work only when the names matches; often time, it is not possible to cross probe from NAV file or XML file to the RTL View.

2. Locating GND and V_{CC} nets.

   When Synplify/Synplify Pro instantiates GND and V_{CC} components, technology view will show "0" and "1" connected to these component, respectively. However, in the EDIF netlist, the nets connected to GND and V_{CC} components are named "GND" and "V_{CC}". Because of this naming mismatch ("0" vs. "GND" and "1" vs. "V_{CC}"), warnings related to "GND" and "V_{CC}" nets can not be cross probed to the Technology View. An example of such warnings are:

   ```
   Logical net 'GND' has no load (WARNING: 454)
   Logical net 'VCC' has no load (WARNING: 454)
   ```

3. If y the corresponding net cannot be located from the NAV file or path/instance from the XML file in the Technology View schematic, click on the "+" sign next to "Net" and scroll down to see if any net is highlighted. If there is a highlighted net, search for the net in other sheets. If no net is highlighted, proceed to the **Troubleshooting** section below.

4. To view only the components connected by the selected net, right click on the schematic window and select **Select Net Instances**. Right click again and select **Filter Schematic**.

5. To cross probe from Technology View to HDL source code, double click on an instance that drives or is driven by the net. The HDL editor window will open and highlight the code that produced the logic.

6. The user can also cross probe from the HDL source code to the RTL View. Highlight the corresponding process in the HDL editor and click on the RTL View window. The

corresponding components will be highlighted. If the user clicks on the Technology View window, the corresponding components should be highlighted as well.

Troubleshooting

When the navigation report (NAV) file or the navigable timing report (XML) file does not cross probe to Synplify / Synplify Pro, there is usually a communication failure between the two applications.

The Error Viewer will prompt the following warning when the communication failed:

```
WARNING:InterToolCommunication:14 - In trying to start the
Synplicity Cross Probing system, the following was returned:

"couldn't open socket: connection refused"

Synplicity Cross Probing will not be enabled.
```

The Timing Analyzer will show the same message in its console window. To view the console window, click on View → Console, then mark the "Show Command Status" checkbox.

The following section describes possible causes and troubleshooting steps when the Error Viewer fails to communicate with Synplify / Synplify Pro.

Incorrect Setup Sequence

When using external cross probing, Synplify / Synplify Pro sets itself up to be the server. This requires that the Synplify / Synplify Pro schematic viewer be opened and the **External Cross Probing Engaged** enabled before the Error Viewer or the Timing Analyzer window is opened. If this sequence is altered, communication between the two applications will not occur. To correct this, simply exit from the Error Viewer or Timing Analyzer window. Make sure the Synplify / Synplify Pro schematic viewer is opened and the External Cross Probing Engaged option is checked. Then, reopen the NAV file in the Error Viewer for logical cross probing or the XML file in Timing Analyzer for timing cross probing.

Conflict on the Port Used for Cross Probing

The environment variables **XIL_ITC_XVENDOR_PORT** and **XPROBE_PORTID** are used to control the cross probing port between the Error Viewer and Synplify / Synplify Pro. These two variables should be set to the same number. When **XIL_ITC_XVENDOR** is set to "synplicity", the default value of the variables is "8000". Leave this variable at the default value unless there is a conflict.

The connection may be refused because the port is being used by another application, such as a license server. The two variables can be set to use another port. To correct this, close Synplify / Synplify Pro and the Error Viewer, then set the two variables to use another port. Once the port environment variables are reset, reopen both applications.

See the following two examples for resetting the port connection:

UNIX Platform:

Type the following commands at the command prompt:

```
setenv XIL_ITC_XVENDOR_PORT <port_number>
setenv XPROBE_PORTID <port_number>
```

PC Platform:

Set the following **autoexec.bat** or system environment setting area. Reboot the PC if using Windows98.

```
set XIL_ITC_XVENDOR_PORT=<port_number>
set XPROBE_PORTID=<port_number>
```

The **<port_number>** is any available TCP/IP port on the local system. A valid port number is a four or five digit integer ranging from 1700 to 65000. Examples of valid values are "8000", "3465", and "15999".

Xprobe_server Not Terminated Properly

When enabling external cross probing, Synplify/Synplify Pro launches a process called "xprobe_server". Occassionally, this process is not terminated properly upon exiting Synplify/Synplify Pro. As a result, the next attempt of external cross probing will not work, although there was no warning about communication failure. To correct this, terminate or kill the old "xprobe_server" process as follows:

UNIX Platform:

- Type "ps" or "top". See whether "xprobe_server" is listed as running process.
- Note the PID number.
- Type the following commands at the command prompt to kill the process:

```
kill -9 <xprobe_server's PID#>
```

PC Platform:

- Press Ctrl-Alt-Del
- Select Xprobe_server task
- Click "End Task"

After terminating the "xprobe_server" process, repeat cross probing sequence from the start.

Cross Probing with Leonardo-Spectrum

This section describes setting up sequence, guidelines, and troubleshooting procedure for cross probing between Xilinx and LeonardoSpectrum schematic viewer.

Setup

The following describes the settings needed to do cross probing with LeonardoSpectrum:

1. The environment variable **XIL_ITC_XVENDOR** must be set to "exemplar". There is no default value for this variable. Setting this variable to "exemplar" specifies that LeonardoSpectrum is the target of the navigation report messages from the error viewer application.

   To set the environment variables, do the following:

   UNIX Platform:

   Type the following command at the command prompt:

   ```
   setenv XIL_ITC_XVENDOR exemplar
   ```

   PC Platform:

   Set the following in the **autoexec.bat** or system environment setting area and reboot the PC if using Windows98.

   ```
   set XIL_ITC_XVENDOR=exemplar
   ```

2. Synthesize the design in LeonardoSpectrum.

3. Set the TCL variable **comm_socket**, which is used to control the TCP/IP port in Exemplar. This variable must be set to "16000" in LeonardoSpectrum.

   To set **comm_socket**, enter the following at the LeonardoSpectrum TCL command line:

   ```
   set comm_socket 16000
   ```

   Note: If using LeonardoSpectrum level 1 or level 2, create a text file with .tcl extension and type the command above into the file (TCL script). To run the TCL script, click **File** → **Run Script...,** select the TCL script, and click **Open**. This will set the comm_socket variable.

The **comm_socket** setting will be saved in the LeonardoSpectrum project (LSP) file when the project is saved. The value will be restored when the project is reopened.

To unset **comm_socket**, enter the following:

```
unset comm_socket 16000
```

To check **comm_socket** value, enter the following:

```
puts $comm_socket
```

4. Save the design project, **File** → **Save Project As**.
5. Implement the design in the Xilinx implementation tools.

   After Translate (NGDBuild) has completed, "**Logical Cross Probing**" can be done.

   After Place-and-Route (PAR) has completed, "**Timing Cross Probing**" can be done.

   Note: With LeonardoSpectrum, only logical cross probing or timing cross probing can be done, but not both at one time.

Logical Cross Probing

To cross probe from the Error Viewer to LeonardoSpectrum, do the following:

1. Invoke the Error Viewer from Design Manager or from the command prompt as described in **Displaying the Navigation Report for Logical Cross Probing**, page 1. The Error Viewer window will show DRC warnings and/or errors from NGDBuild with the net names highlighted, as shown in Figure 12.

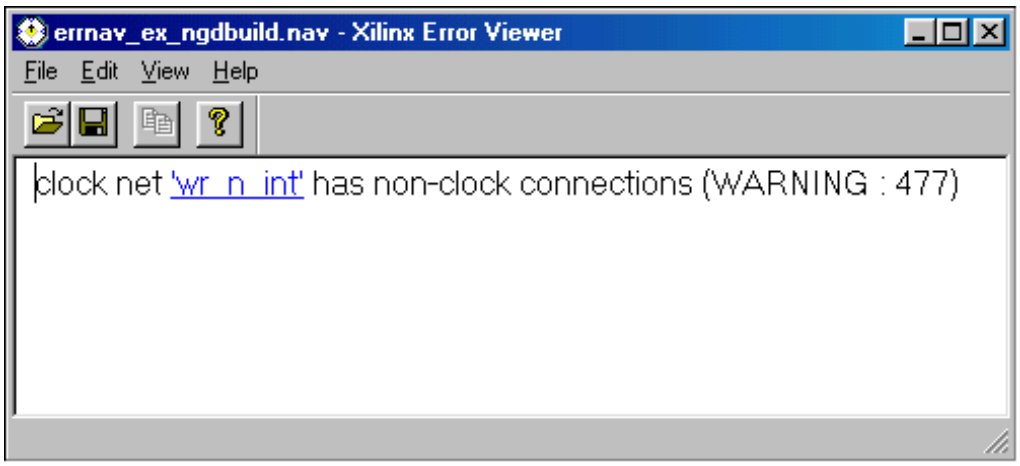


Figure 12: **Navigation Report from LeonardoSpectrum Synthesized Design**

2. Open the design project (LSP) file in LeonardoSpectrum.
3. Make sure the TCL variable **comm_socket** is set. See "**Setup**" section.
4. Select **Tools** → **Connect to External Tool**. The following message appears if the connection was successful:

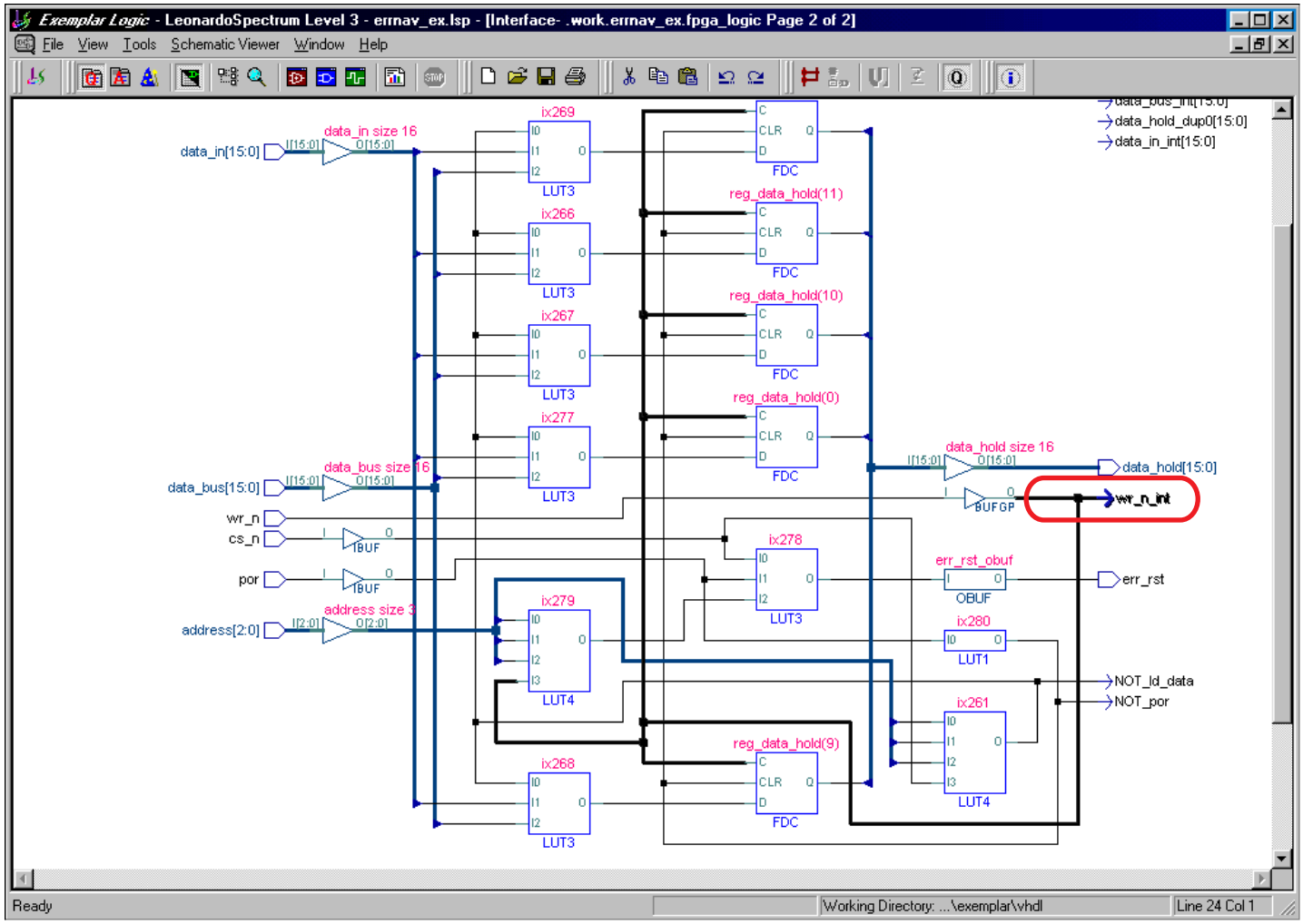
   ```
   xmplr_send_msg $xmplr_socket "Connected to
   LeonardoSpectrum"
   ```

   If the connection failed, the following message will appear:

   ```
   couldn't open socket: connection refused
   ```

   See **Troubleshooting**, page 16, if the socket fails to open and no connection is made.
5. OPTIONAL: Select **Tools** → **View RTL Schematic**.

6. Select **Tools** → **View Gate Level Schematic**.
7. Click on a net in the Error Viewer window. The corresponding net should be highlighted in the Gate Level Schematic window as shown in Figure 13, page 13.



X406_06_083100

Figure 13: **Highlighted in the Schematic Window: Net `wr_n_int`**

Timing Cross Probing

To cross probe from the Timing Report in Timing Analyzer to LeonardoSpectrum, do the following:

1. Display the XML file as described in **Displaying the Navigable Timing Report for Timing Cross Probing**, page 2. The timing report in the Timing Analyzer window will show navigable paths and instances as shown in Figure 2

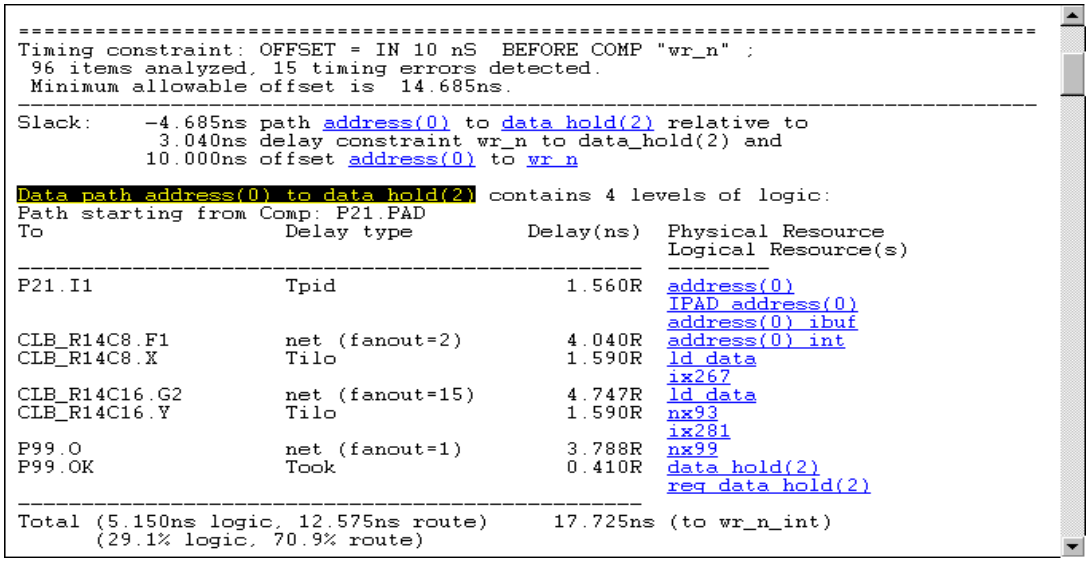


Figure 14: **Path Selected to Cross Probe to LeonardoSpectrum Schematic Window**

2. Click on a path or an instance once. This will enable cross probing for Timing Analyzer.
3. Open the design project (LSP) file in LeonardoSpectrum.
4. Make sure the TCL variable **`comm_socket`** is set. See "**Setup**" section.
5. Select **Tools** → **Connect to External Tool**. The following message appears if the connection was successful:

   ```
   xmplr_send_msg $xmplr_socket "Connected to
   LeonardoSpectrum"
   ```

   If the connection failed, the following message will appear:

   ```
   couldn't open socket: connection refused
   ```

   See **Troubleshooting**, page 16, if the socket fails to open and no connection is made.
6. OPTIONAL: Select **Tools** → **View RTL Schematic**.
7. Select **Tools** → **View Gate Level Schematic**.
8. Click on a path or an instance in the timing report to cross probe. he corresponding net should be highlighted in the Gate Level Schematic window as shown in Figure 13, page 13. See the **Locating Nets and Instances in the Schematic View** section if the path is not highlited.

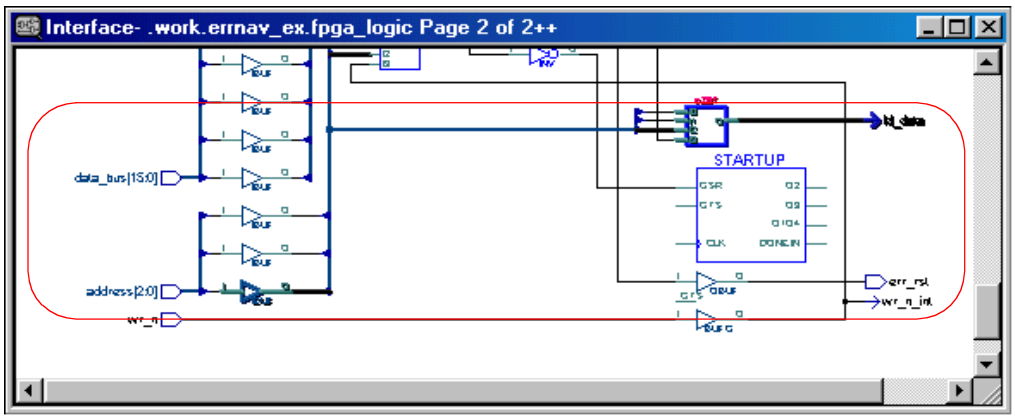


Figure 15: **Selected Path Highlighted in LeonardoSpectrum Gate Level Schematic**

9. To isolate the schematic to show only the selected path, right click on the **Gate Level View** window and select **View Trace Schematic**. The filtered path is shown in Figure 11.

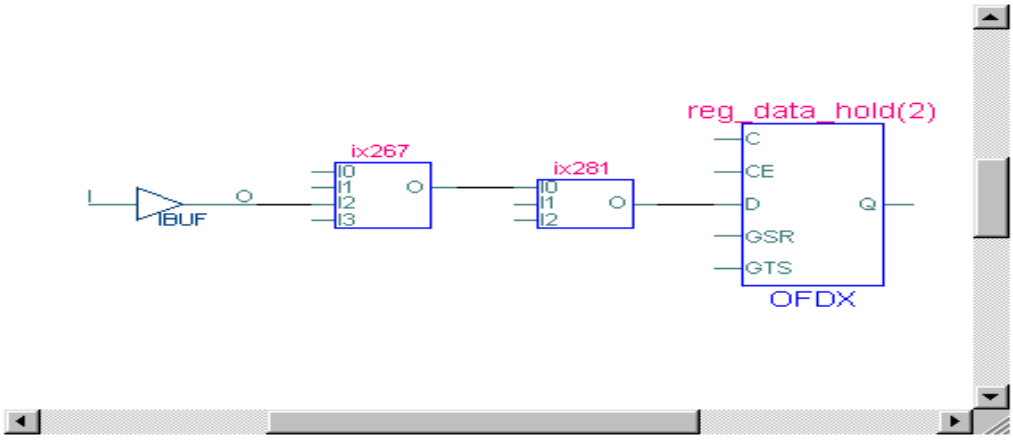


Figure 16: **Filtered Path in LeonardoSpectrum Gate Level Schematic**

Locating Nets and Instances in the Schematic View

The following are guidelines on how to locate a net/path/instance in LeonardoSpectrum:

1. Make sure LeonardoSpectrum version 2000.1b and later is used. The earlier version of LeonardoSpectrum can not communicate the information needed to do timing cross probing with Xilinx.
2. Most instances/nets/paths can cross probe only to the Gate Level Schematic.

   In LeonardoSpectrum, net and instance names are altered in synthesis during technology mapping. This causes the names in the RTL Schematic to differ from the names in the Gate Level Schematic. On the other hand, Xilinx Implementation tools get the net/instance names from the EDIF netlist which are identical to the names in the Gate Level Schematic. Since the logical and timing cross probing work only when the names matches; often time, it is not possible to cross probe from a NAV file or an XML file to the RTL Schematic.
3. Cross probe from the Gate Level Schematic to HDL source code by right clicking on a component that drives or is driven by the net, and select **Trace to HDL Source**. The HDL Editor window displays. The code that produced the logic will be highlighted.
4. To view only the components connected by the selected net, right click on the Gate Level Schematic window and select **View Trace Schematic**

Troubleshooting

When the navigation report (NAV) file or the navigable timing report (XML) file does not cross probe to LeonardoSpectrum, there is usually a communication failure between the two applications.

Incorrect Setup Sequence

The following message appears in the LeonardoSpectrum information window:

```
Attempting to connect to host: 127.0.0.1 on port:16000
couldn't open socket: connection refused
```

When connecting to the external tool, LeonardoSpectrum expects the external tool to be the server. This requires the external tool, in this case the Error Viewer or Timing Analyzer to initialize the cross probing before **Connect to External Tool** is enabled. See **Logical Cross Probing** or **Timing Cross Probing** section for the correct sequence. If the sequence is altered, the communication between the two applications will not occur.

To correct this for **logical cross probing**, do the following:

1. Close and reopen the Error Viewer.
2. Select the **Tools** → **Reconnect to External** tool from the LeonardoSpectrum menu.
3. Continue from Step 5 of **Logical Cross Probing** section.

To correct this for **timing cross probing**, do the following:

1. Close and reopen the Timing Analyzer.
2. Open the XML file in the Timing Analyzer window
3. Click on a path/instance to initialize timing cross probing.
4. Select the **Tools** → **Reconnect to External** tool from the LeonardoSpectrum menu.
5. Continue from Step 6 of **Timing Cross Probing** section.

`Comm_socket` Is Not Set

The following message appear in LeonardoSpectrum information window:

```
xmplr_socket_init
can't read "comm_socket": no such variable
```

The environment variable **`XIL_ITC_XVENDOR_PORT`** and TCL command **`set comm_socket`** are used to control the cross probing port between the Error Viewer and LeonardoSpectrum. These variables and commands should be set to the same number. When **`XIL_ITC_XVENDOR`** is set to "exemplar", the default value of **`XIL_ITC_XVENDOR_PORT`** is "16000". However, there is no default value for **`comm_socket`**. To correct this, set the comm_socket as described in **Setup** section.

Conflict on the Port Used for Cross Probing

The connection may be refused because the default port "16000" is being used by other application, such as a license server. **`XIL_ITC_XVENDOR_PORT`** and **`comm_socket`** can be st to another port.

To correct this, do the following:

1. Close the Error Viewer or Timing Analyzer window.
2. Set **`XIL_ITC_XVENDOR_PORT`** to use another port:

   UNIX Platform:

   Type the following command at the command prompt:

   `setenv XIL_ITC_XVENDOR_PORT <port_number>`

   PC Platform:

Set the following in **autoexec.bat** or the system environment setting area and reboot PC if using Windows98.

```
set XIL_ITC_XVENDOR_PORT=<port_number>
```

The ***<port_number>*** is any available TCP/IP port on the local system. A valid port number is a four or five digit integer ranging from 1700 to 65000. Examples of valid values are "8000", "3465", and "15999".

3. Follow the sequence in the **Logical Cross Probing** or **Timing Cross Probing** section, but set **comm_socket** to match **XIL_ITC_XVENDOR_PORT** in LeonardoSpectrum's TCL prompt:

```
set comm_socket <port_number>
```

Known Issues

Below is the list of the current known issues for the Error Viewer.

1. When the cursor is pointing to the highlighted net in the Error Viewer, it does not change to a link selector cursor.
2. After clicking the highlighted net in the Error Viewer, the highlight does not change color to indicate that it has been selected.
3. Using an environment variable to control the Error Navigation setting is inconvenient for Windows98 platform users. A switch or UCF control will be added in a future software release.

New known issues will be logged in the Xilinx Answer Database accessible from http://support.xilinx.com. Cross probing related issues can be searched using "cross probing" keywords.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/01/00	1.0	Initial Xilinx release.
12/01/00	2.0	Title changed, includes logical and timing cross probing.