Implementing an I²C Bus Controller in a *CoolRunner* CPLD

Here's an overview of a complete design that you can download from the Web.

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The I²C bus is a popular serial, two-wire interface used in many systems because of its low electrical overhead. The two-wire interface minimizes interconnections so ICs have fewer pins and the number of traces required on printed circuit boards is reduced. The bus is capable of up to 100KHz operation, and each device connected to the bus is software addressable by a unique address with a simple master/slave protocol.

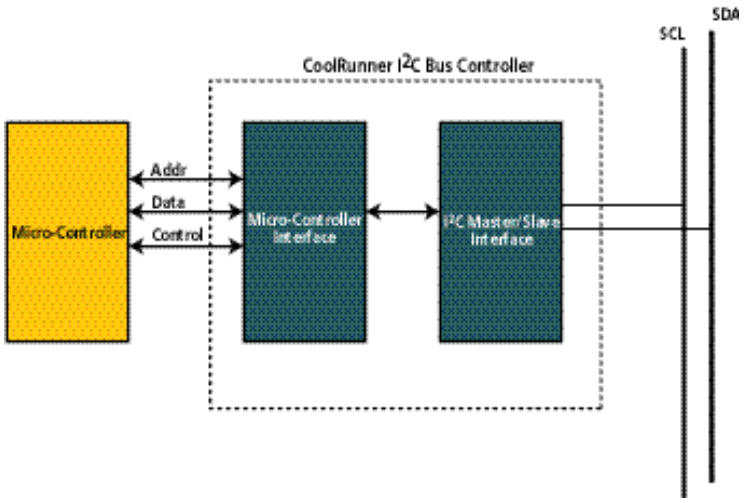

Figure 1 - CoolRunner I²C Bus Controller.

Designing with an I²C bus for handheld devices requires that you minimize power dissipation. That's why CoolRunner CPLDs, the lowest power CPLDs available, are the perfect devices for creating I²C controllers. The I²C design shown in this article provides both master/slave capability with an asynchronous byte-wide microcontroller or microprocessor interface as shown in Figure 1.

Functionality

The CoolRunner CPLD implementation of the I²C controller supports the following features:

- Microcontroller interface.
- Master or Slave operation.
- Multi-master operation.
- Software selectable acknowledge bit.
- Arbitration of lost interrupts with automatic mode switching from Master to Slave
- Calling address identification interrupt with automatic mode switching from Master to Slave.
- START and STOP signal generation/detection.
- Repeated START signal generation.
- Acknowledge bit generation/detection.

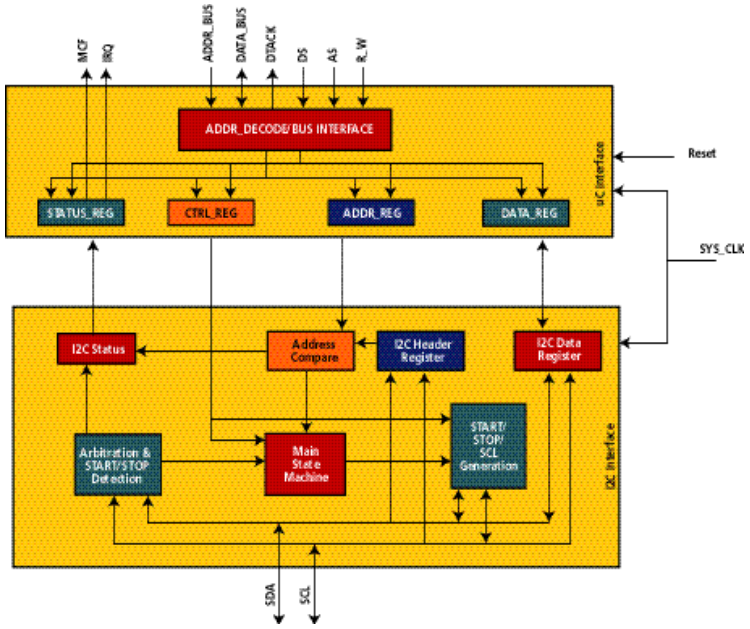

Figure 2 - CoolRunner I²C Controller block diagram.

- Bus busy detection.
- 100KHz operation.

Block Diagram

The functionality of the CoolRunner I²C controller is divided into two major blocks, the microcontroller interface and the I²C interface, as shown in Figure 2. This design was created in VHDL and verified through simulation. Xilinx software tools were used for compilation and fitting. The design was targeted to a 3V, 128-macrocell, enhanced clocking, CoolRunner CPLD in a 100-pin TQFP package (XCR3128A-10VQ100C).

Conclusion

This design offers a way to use an I²C bus in a low power application. Using a CoolRunner CPLD to implement the functionality of an I²C controller is perfect for power limited applications. The design of the I²C controller that is currently available for customers includes the following:

- Complete detailed application note
- Complete VHDL source code
- VHDL test benches

More information can be found at www.xilinx.com/apps/epld.htm,under CoolRunner XAPP315 - Implementing an I²C Bus Controller in a CoolRunner™ CPLD. The VHDL code and test benches created for this design are available by contacting Xilinx Technical Support at 1-800-255-7778.