ModelSim™

Using the ModelSim FPGA Library Manager

Using the new FPGA Library Manager will improve your simulation time by easily building Xilinx FGPA libraries for use within ModelSim.

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ModelSim is a mixed-language, single-kernel simulator, allowing you to simulate Xilinx FPGA instances implemented in Verilog, together with other instances in VHDL, in the same simulation run. You have flexibility in your choice of HDL language, and you can easily build the simulation library for your chosen Xilinx FPGA (and HDL language) with the FGPA Library Manager which supports simprim, unisim, and LogiBLOX simulation libraries in both Verilog and VHDL for all Xilinx FPGA families.

Using the FPGA Library Manager

The new ModelSim FPGA library manager guides you through the process of compiling the FPGA libraries provided by Xilinx. These compiled libraries can then be used with your design to simulate with ModelSim. The source code for the Xilinx libraries is included with the Alliance Series Software, and is referenced by the "XILINX" Environment Variable.

Here are step by step instructions for using the Library Manager:

- Invoke ModelSim and go to a working directory where you want to compile the FPGA libraries (this can be where your design source files are located). A welcome banner will appear. This new banner contains several new features, including a new Project Wizard. The Project Wizard is documented in the ModelSim Reference Manual, and in the Tutorial which has an example project. Dismiss the Welcome Banner, continue to ModelSim.
- From the main ModelSim window change directories. Use **File > Change Directory** to Browse for your working directory
- From the main window command line enter: **vlib work**
- Select the FPGA Library Manager which will build the FPGA library. Use **Design > FPGA Library** Manager.
- Use the Browser to select the Xilinx TCL script. (ModelSim uses TCL as a scripting language.) The Library manager uses a support file that resided in the ModelSim_install_directory/contrib. These scripts will be updated as the Xilinx parts list evolves. See the Additional Information section below for updated script downloads. Use **Browse > Select fpgavendor_xilinx.tcl > Open > Next** (Please refer to Figure 1 "ModelSim XILINX FPGA Library Manager Window".)
- Select a ModelSim project initialization file

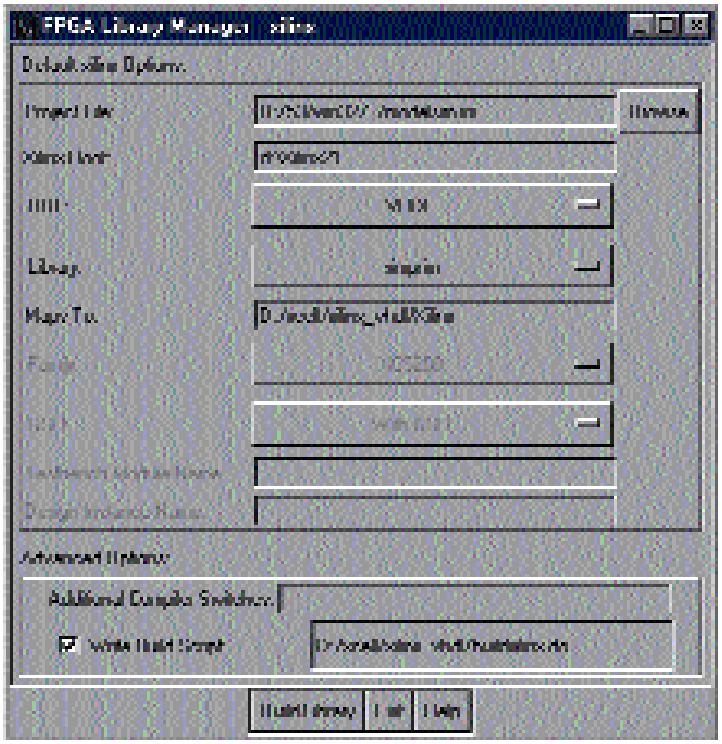

Figure 1: ModelSim Xilinx FPGA library manager window.

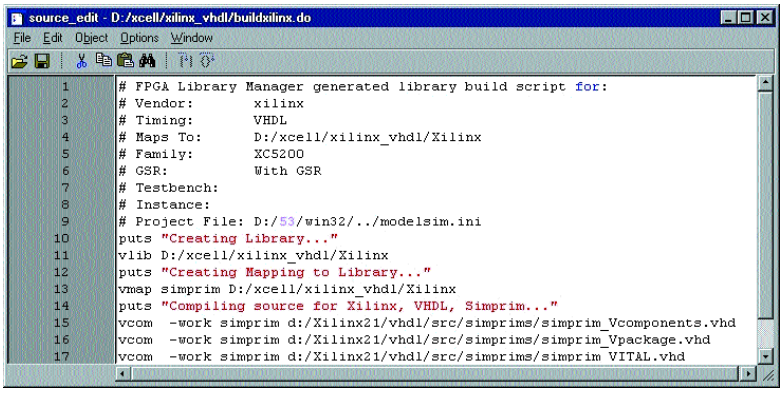

Figure 2: ModelSim Xilinx FPGA library script.

(which contains default settings for ModelSim). The Xilinx root directory value is from your system environment variables.

- Choose your HDL language (VHDL or Verilog). If you have a VHDL testbench, you can run a Verilog description of your design with ModelSim, if the pin names match exactly (d[0:31] does not match d1,d2....d31) and you are using STD LOGIC at the IO (ModelSim will map VHDL to Verilog strength).
- Select the Xilinx FPGA Library. The Xilinx Library source code that gets compiled is from the Xilinx root directory, which is read from your system environment variable. The example uses the XC5200 Family. The Maps To entry is a name of the ModelSim library you wish to use. This can be any name you wish, default is XILINX. This physical name can be mapped to the needed logical name required by the source code.
- Select **Write Build Script**; the default path name is the current directory. (ModelSim is a full featured simulation tool that can be run in UI mode, command line mode, or batch mode. The ModelSim FPGA Library Manager can create a script that can be used to re-compile the FPGA library.) The TCL script can be seen in Figure 2: the vlib command creates a ModelSim library, vcom is the VHDL compiler, and

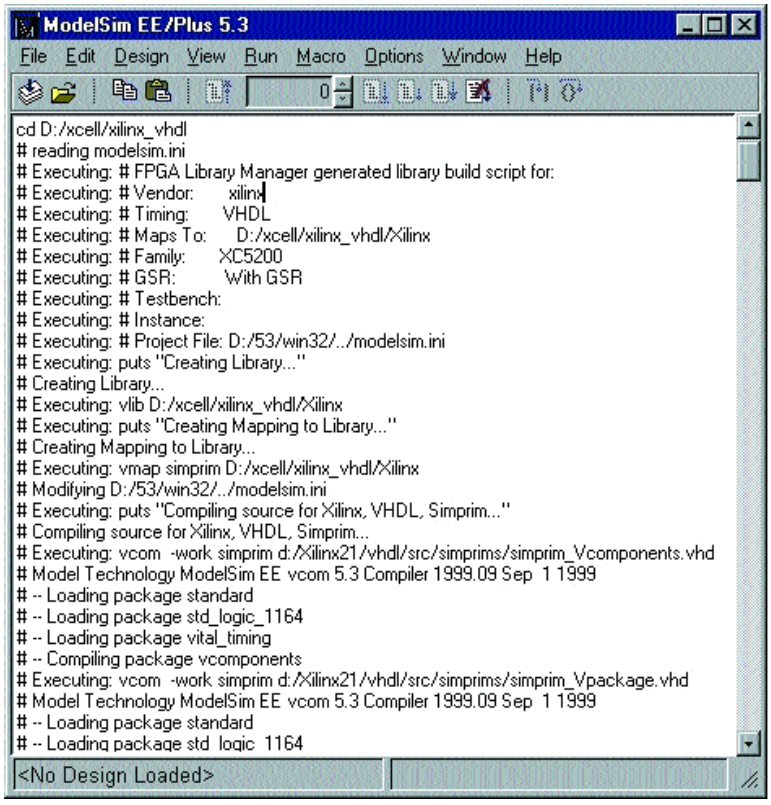

Figure 3: Main ModelSim window.

vmap maps the physical location to the logical name used in your VHDL source code. This script can now be used to build the library without the use of the FPGA Library Manager. See the MTI Application Notes for a full description of the use of scripts with ModelSim.

- Select **Build Library**. The Main Window scrolls messages indicating the library has been built as shown in Figure 3. When the library compilation is complete an information window will appear. Dismiss the library compiled information window, and Exit the FPGA Library Manager. The ModelSim build script is shown in Figure 2.

Main Window -> Open ->Open Source, select buildxilinx.do.

The library is now available for use with your source files.

Additional Information

For updates to the Xilinx FPGA vendor compile scripts, go to:

http://www.model.com/resources/fpgalibmgr.html

For a complete Application Note ModelSim 5.2 With Xilinx Alliance 2.1 showing step by step instructions for using ModelSim to compile and simulate any of your Xilinx designs, go to:

http://www.model.com/pdf/113_xilinx_21.pdf

For a list of all MTI Application Notes, including ModelSim 5.2 with Alliance 1.5, and example circuits for use with Application Notes, go to:

http://www.model.com/support/technote/index.html

Conclusion

The new ModelSim FPGA library manager removes the question of how to compile the Xilinx FPGA libraries, so you can focus on the verification of your Xilinx design.