Fast Zero Power (FZP) Technology

How CoolRunner CPLDs Minimize System Current Demand

CoolRunner CPLDs require very little power yet operate at very high speeds—here's how.

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In traditional CPLD architectures, including the XC9500 series, the circuits that propagate logic-level transitions in the product-term array are derived from the original (old) bipolar PLD designs. These older designs use sense amplifiers at the end of each bit line in the product-term array to achieve fast propagation delays. Because CPLD product terms cannot be decoded (as with memory locations in an EPROM, for example) there must be a sense amplifier for each individual product-term. These sense amplifiers must be continuously operational, and will draw continuous supply current even when not switching.

The CoolRunner Design Technique

The Xilinx CoolRunner design uses an innovative method for implementing the product-term array. Rather than employing sense amplifiers (a bipolar-style circuit), CoolRunner CPLDs use true CMOS circuitry. In the CoolRunner Fast Zero Power (FZPTM) approach represented in Figure 1, the AND gates in the product-term array are implemented using configurable multiplexers (MUXs) attached to the inputs of normal CMOS NAND gates. Each MUX selects an input, it's complement, or Vcc (don't care state.) These MUXs are programmed using RAM-based configuration bits.

The full CMOS AND gate shown in Figure 1 has a delay of under 0.5 nsec, including the delay of the input MUXs.

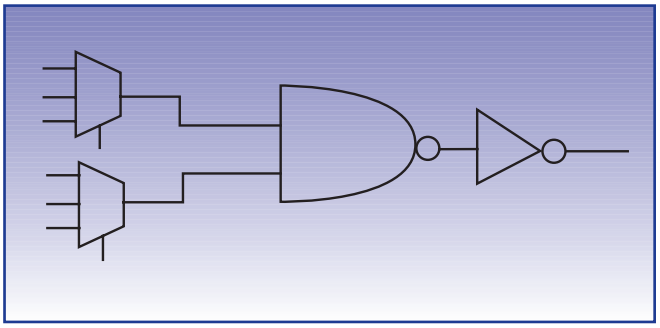

Figure 1 - CoolRunner Fast Zero Power AND gate.

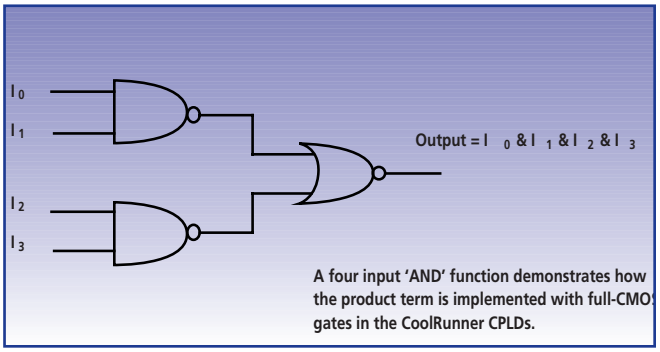

Figure 2 - Representation of a 4-input product-term using the CoolRunner FZP design technique.

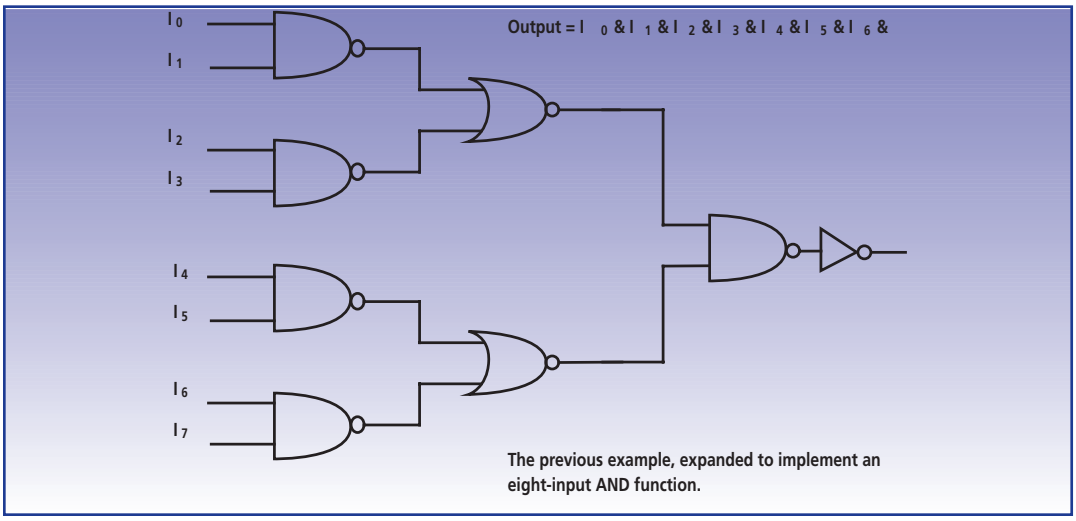

Figure 3 - Expanding the number of inputs.

Wider AND gates are built using a deMorgan tree, as shown in Figure 2. Doubling the input width simply requires the replacement of the inverter in Figure 1 with a 2-input NOR gate. This increases the total delay by less than 0.1 nsec.

This design technique can be extended for wider widths, as shown in Figure 3 which shows a re-doubling to eight inputs, at an additional delay penalty of less than 0.2 nsec for the NAND gate plus inverter. The inverter can be replaced with a two-input NOR gate to enable a product-term width of 16 inputs (at an incremental delay penalty of 0.1 nsec.).

As you can see, the delay penalty per additional input actually decreases as the number of inputs into each product-term increases. This is in contrast to the traditional sense amplifier approach, where the delay increases linearly as product-term input width is increased.

The gate tree implementation distributes the capacitance at each product-term, so this capacitance is no longer lumped on a single node. Furthermore, the switching current behaves in a manner similar to that of random logic in a gate array; the static current for each gate is small-about 1 picoamp (pA). The total instantaneous dynamic current is also small, because only the gates in one path of the tree can switch, and these gates switch in succession rather than all at once.

Conclusion

The advantages of CoolRunner FZP CPLDs are numerous. Total standby current is under 100 microamps—at least 1000 times less than that exhibited by CPLDs using sense amplifiers. Total dynamic power is also decreased, relative to existing CPLDs, by as much as 70% for a device whose logic is fully populated with 16-bit counters operating at 50 MHz. Best of all, these power savings are realized with little impact on performance and with no cumbersome power-down circuitry.

Because power consumption is so low, chip-scale packaging options, once considered impossible due to thermal limits, are now offered. As a result, FZP technology is a key technology for CPLDs because it enables very low-power, high-performance applications. Σ