Design Technology Advances Unleash Powerful New FPGA Capabilities

The Chief Technology Officer at Synplicity talks about the trends that are shaping the FPGA industry.

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In today's marketplace there is enormous pressure to create increasingly complex systems and get those systems to market as quickly as possible. To challenge these efforts, there is a lack of qualified engineers, industry standards are constantly changing, ASIC development costs are skyrocketing, and new technologies are quickly making yesterday's methods obsolete. These problems are intensified with the fierce competition for lucrative emerging markets. The risks are significant; one equipment vendor estimates the cost of missing a market window to be more than $1 million a day.

However, there is also good news. Today's multi-million gate FPGAs offer great promise for designers confounded by the limitations of traditional ASIC implementation. Indeed, the increased

time-to-market demands and lower development cost of FPGAs, combined with today's FPGA capacities well in excess of a million gates, are yielding a profound increase in the number of applications being realized in programmable form. From networking and telecommunications designers grappling with narrow market windows and evolving standards, to a broad scope of designers seeking low-risk rapid prototyping, the number of people turning to FPGA solutions is quickly expanding.

Engineers Designing both FPGAs and ASICs

Only six years ago, engineers were divided into two distinct groups: those that designed ASICs and those that designed with FPGAs. The FPGA designers were primarily schematic based while the ASIC designers had adopted RTL technologies. These two groups didn't work together.

Today, things have changed. Many designers developing FPGAs are also designing ASICs, often at the same time. In addition, designers are now less concerned about the underlying device technology because the gap between ASIC and FPGA performance is narrowing. However, ASICs will remain the technology of choice for certain types of applications. If a design must operate at the low end of power consumption or at the extreme upper end of performance, or if you are designing a very high-volume, cost-sensitive system, an ASIC is likely the most cost-effective solution. If design flexibility or remote design upgradability are needed or if engineering time and risk must be minimized, an FPGA is a logical choice.

The SoC Opportunity for FPGAs

The advent of systems on chips (SoCs) is more than a simple extension of ASIC technology to higher density. With SoCs, ASIC designers have become system designers, and the event-driven simulation technology traditionally used is no longer sufficient for verifying functionality. Instead, what designers urgently need is a faster, higher-level, hardware-oriented verification path that accepts actual system inputs to yield actual system outputs. Fortunately, just such an approach exists in RTL prototyping, a methodology being adopted widely by both ASIC vendors and system houses.

In contrast to conventional ASIC designers who tend to focus on the functions within their chips, SoC designers must give much more consideration to the system-level nature of the device's inputs and outputs.

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Software simulation, which checks circuit functionality against a blast of test vectors, falls short of allowing system I/O to be tested. Other drawbacks of software simulation are well known; it is too slow and can't reproduce electromechanical interactions such as fetching data from a drive. Simulation can take as much as 60 percent of the design cycle time and require too many iterations between RTL and gate-level implementation. Also, it does not allow for co-verification of hardware and software.

These roadblocks stand in the way of what SoCs require. For example, consumer and communication designs (areas of great promise for SoCs) compete within tight time-to-market windows that suffer when debugging takes many iterations through long cycles of simulation and synthesis. In addition, many chips for these markets must run at high clock rates to verify their correct operation. Inadequate verification of these designs can mean one or more fab re-spins, which can cost over $1 million per re-spin and take up to six months.

To take fuller advantage of the SoC phenomenon, designers can instead turn to RTL prototyping, a new methodology that is possible through the emergence of fast, dense FPGAs such as the Xilinx Virtex FPGAs and synthesis technologies that can translate ASIC RTL into multiple FPGAs. By building a version of their design in hardware using multiple FPGAs, designers can use RTL prototyping to leapfrog all of the limitations of software simulation.

FPGAs Offer Design Flexibility

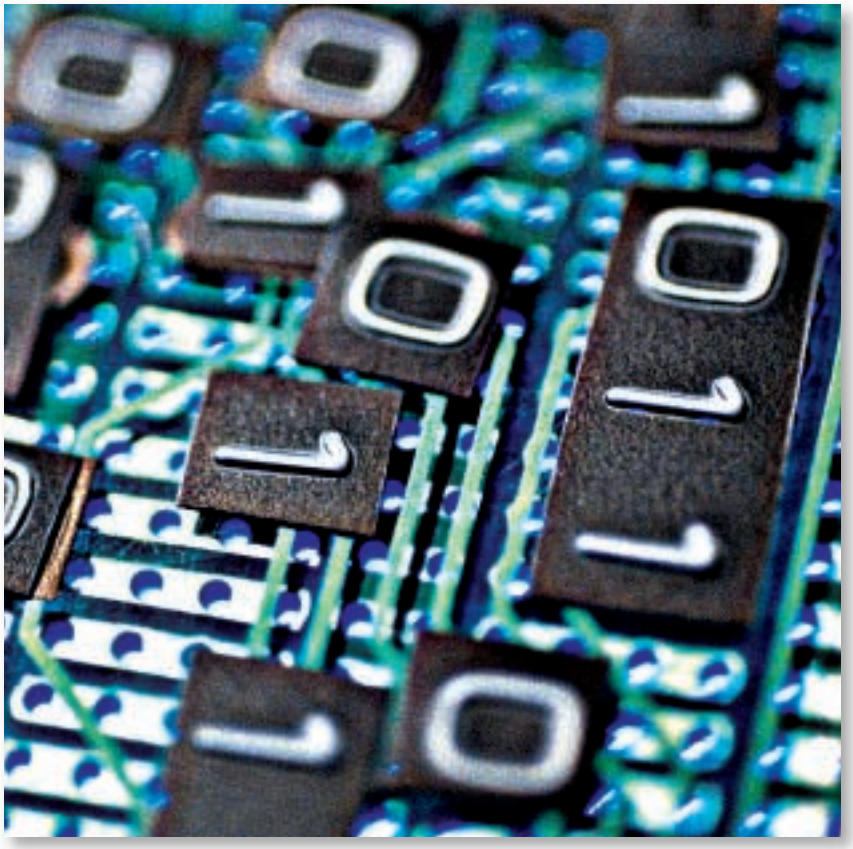
The Internet's explosive popularity, and the resulting surge in demand for bandwidth, has created immense competitive pressure for communications equipment makers. To complicate matters, the communications market is a minefield of specifications evolving unpredictably toward standardization. Schemes for carrying voice and video over the Internet, or the Internet over cable, or any number of variations on the Internet theme bring with them a multitude of implementation details that often must either be ironed out by committees or decided by the market.

Such last minute unpredictability makes bringing complex communications equipment to market quickly even more difficult. Equipment vendors who hope to exploit the high-density and high-volume economics of ASIC technology risk everything should a last minute protocol change force a silicon re-spin. Realizing this, increasing numbers of equipment manufacturers are instead opting for the fast turnaround and flexibility offered by FPGAs.

The quick re-configurability of FPGAs carries other benefits in addition to accommodating shifting specifications. By exploiting the option for in-system programmability, companies can easily and affordably make field upgrades, correct bugs and add features over the Internet, to name just a few possibilities.

The Impact of FPGA Technology Advances

FPGA technology used to be one or two generations behind ASICs. However, the increase in FPGA density and performance has steadily outpaced that of ASICs for some time. Because of the increasing NRE costs of leading-edge ASICs, the typical ASIC design is falling farther behind the leading edge of process technology, while FPGAs are becoming process drivers.



However, taking full advantage of state-of-the-art FPGA technology today presents new and difficult challenges. As FPGA process technology progresses well into the deep submicron realm, interconnect-dominant delay now poses the same difficulties for FPGA designers that previously plagued their ASIC counterparts. Traditional schematic or logic synthesis-based programmable design solutions, similar to the ASIC methodologies of three to four years ago, lack the ability to adequately account for interconnect effects early in the design cycle. With today's highly complex circuits and relentless market pressure, it is more important than ever that accurate interconnect-related performance information be integral to early design processes.

Evolution of Software

Design automation is key to enabling this new era of FPGA design. Unfortunately, simply extending interconnect-aware ASIC design technology to the FPGA domain won't work. The interconnect configurations and options unique to FPGA architectures cannot be comprehended utilizing ASIC physical modeling techniques. Instead, new FPGA-targeted design automation technology is needed. Such technology must address the difficult task of bringing accurate information about the physical interconnection of a programmable circuit into the design process without extending design cycles.

Fortunately, FPGA design technology is evolving to accommodate the needs of designers in the deep submicron era. Of particular significance is FPGA-based physical synthesis technology. Physical synthesis factors a design's physical characteristics into the synthesis process. During synthesis, a design is optimized and implemented based upon not only traditional timing constraints, but also physical constraints. The nature of FPGA architectures makes it possible to perform physical optimization techniques during synthesis, for example, moving registers across regional boundaries to increase performance.

Physical synthesis offers significant productivity as well as performance advantages to FPGA designers. First, the use of physical constraints during synthesis results in more accurate timing estimation, eliminating time-consuming and tedious design iterations common with traditional approaches. Likewise, physical optimization during synthesis makes it possible to physically optimize a circuit for the best possible performance. Combined physical synthesis and optimization techniques can have significant cost benefits, enabling designers in many cases to implement a device in a lower-cost speed grade.

FPGA physical synthesis forms the critical link between state-of-the-art programmable technology and designers seeking to leverage its unique advantages. Such technology opens the door of opportunity for those faced with today's tough market realities.

Conclusion

Market forces have created a risky environment where the winners and the losers are often separated by only a small gap of innovation. Therefore, it is increasingly important to produce next-generation designs on time and within budget, using limited engineering resources. Today's programmable logic technology and the development tools that support them are your keys to success in this dynamic marketplace.