StateCAD XE for Optimizing State Machine Design

Now you can implement faster, more compact state machines, with ease.

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Control logic is usually implemented as finite state machines (FSMs), which usually require you to work through multiple levels of design and optimization, often within tight development schedules. And, as designs grow larger, the complexity of implementing control logic increases correspondingly, forcing you to migrate from schematics to hardware description languages (HDLs). StateCAD® XE automates the state machine development process, saving you a lot of time and trouble.

Manual FSM Design

Until recently, you had to specify control logic manually; you had to draw state diagrams by hand (or with a graphics package), and then manually translate them to schematics or to an HDL. Timing and logic problems identified during simulation resulted in modifications to the original design, which then needed to be re-verified, step-by-step.

This approach tends to be slow, repetitive, and error-prone. Translation errors invariably creep in and require substantial effort to eliminate.

Hardware Description Languages (HDLs) allow more logic to be specified and maintained with less effort, and they can be synthesized in numerous ways. You can control how synthesis operates, allowing you to create your design in the manner best suited to your target application.

The way an HDL is structured dramatically impacts the speed, area, and power consumption of the synthesized device. When doing finite state machine design, the best results can only be achieved by careful consideration of the resources available, and by having the flexibility to experiment with different alternatives.

Automated FSM Design Using StateCAD XE

A quicker way to implement state machines optimized for Xilinx devices is to use the Xilinx ISE software, which includes StateCAD XE. This tool allows you to draw complex state diagrams, choose design specific optimizations, and generate synthesizable VHDL, Verilog, or Abel-HDL. StateCAD allows you to change optimizations (including state assignment mode, registering output, and signal loading), then reproduce the HDL automatically.

One advantage of automatic state machine translation is the ability to change optimizations and regenerate code in seconds. By trying different code styles, state assignment modes, and optimizations, you can find which combination yields the optimal solution for your design.

State Machine Example

By comparing implementations of a simple state machine, we can see the impact on state machine design. The small state machine in Figure 1 will be implemented with both registered and combinatorial outputs, illustrating the impact of output optimization on implementation:

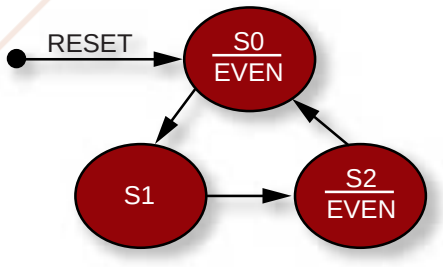

Figure 1 - Example state machine

Output Optimization

Outputs can be optimized for speed (registered) or for area (combinatorial decode). Combinatorial decoded outputs become active by decoding state registers (Moore) or by decoding state registers and inputs (Mealy). Registered outputs are calculated prior to the active edge of the clock, and typically improve speed because a level of propagation delay is removed, but usually require more area than combinatorial implementations. Registered outputs are insensitive to input glitches or to multiple state bit changes.

Design Results

In Table 1 you can see the registered design has outputs that change at the same time as the state bits, and are stable between clocks. The output delay time is the clock to output delay of the register. All decoding necessary for the output occurs before the clock, at the same time as the decoding for the next state. The decode time is effectively "buried" in the state decode time, producing a faster design.

In comparison, the combinatorial design requires time to decode the state bits, yielding a slower implementation. The advantage for the combinatorial design is the smaller area: 5 logic elements compared to 8 for the registered design.

REGISTERED OUTPUTS

```
PROCESS (sreg, RESET) BEGIN
   next_EVEN <= '0'; next_sreg<=S0;
   IF ( RESET='1' ) THEN
      next_sreg<=S0; next_EVEN<='1';
   ELSE
      CASE sreg IS
         WHEN S0 =>
next_sreg<=S1;
         WHEN S1
=> next_sreg<=S2; next_EVEN<='1';
         WHEN S2 => next_sreg<=S0;
next_EVEN<='1';
      END CASE;
   END IF;
END PROCESS;
```

COMBINATORIAL OUTPUTS

```
PROCESS (sreg, RESET) BEGIN
   EVEN <= '0'; next_sreg<=S0;
   IF ( RESET='1' ) THEN
      next_sreg<=S0; EVEN<='1';
   ELSE
      CASE sreg IS
         WHEN S0 => next_sreg<=S1;
EVEN<='1';
         WHEN S1 => next_sreg<=S2;
         WHEN S2 => next_sreg<=S0;
EVEN<='1';
      END CASE;
   END IF;
```

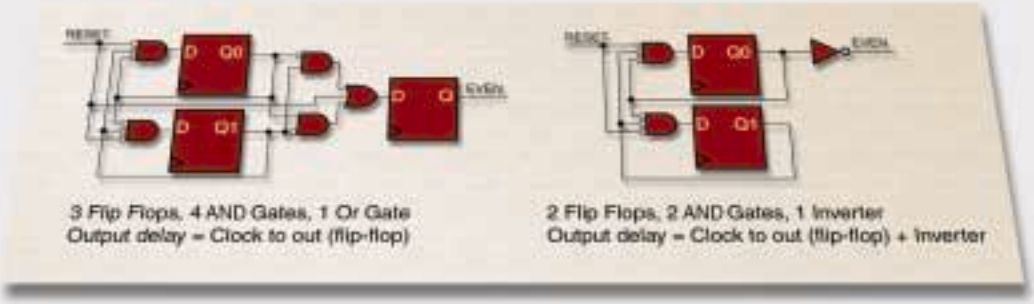

Table 1 - Comparison of output styles

Additional StateCAD Benefits

StateCAD provides additional benefits to Xilinx customers:

- By automating the complete state machine development process, the Xilinx ISE software and StateCAD eliminate manual coding, translation errors, stale documentation, and logic bugs.
- StateCAD includes wizards tailored for designing concurrent state machines and associated logic. State diagrams can include states, transitions, Mealy and Moore outputs, resets, counters, shifters, multiplexers, and much more. No HDL knowledge is required to specify control flow.
- StateCAD exhaustively analyzes state diagrams for inconsistencies, automatically identifying more than 200 problems, such as stuck-at-states, conflicting outputs, and non-deterministic control flow.
- StateCAD includes a built-in simulator called StateBench, for behavioral verification and identification of problems at the state diagram level.
- StateCAD automatically translates state diagrams to synthesizable VHDL and Verilog. Optimizations include one-hot state assignment, registered outputs, and prioritized transitions.
- StateCAD is fully integrated within the Xilinx ISE software, and produces HDL optimized for Xilinx devices, guaranteeing you the best possible results.
- StateCAD can import FSMs created with previous releases of the Xilinx Foundation Series software.

Conclusion

Using StateCAD XE you can quickly implement state machines optimized for Xilinx devices. As design parameters change, just select a new set of optimizations, then regenerate code suited for the new requirements.

StateCAD XE is available at no charge to Xilinx customers, and is included with the Xilinx ISE software or can be downloaded from www.xilinx.com (download StateCAD from the WebPack BackPack section).