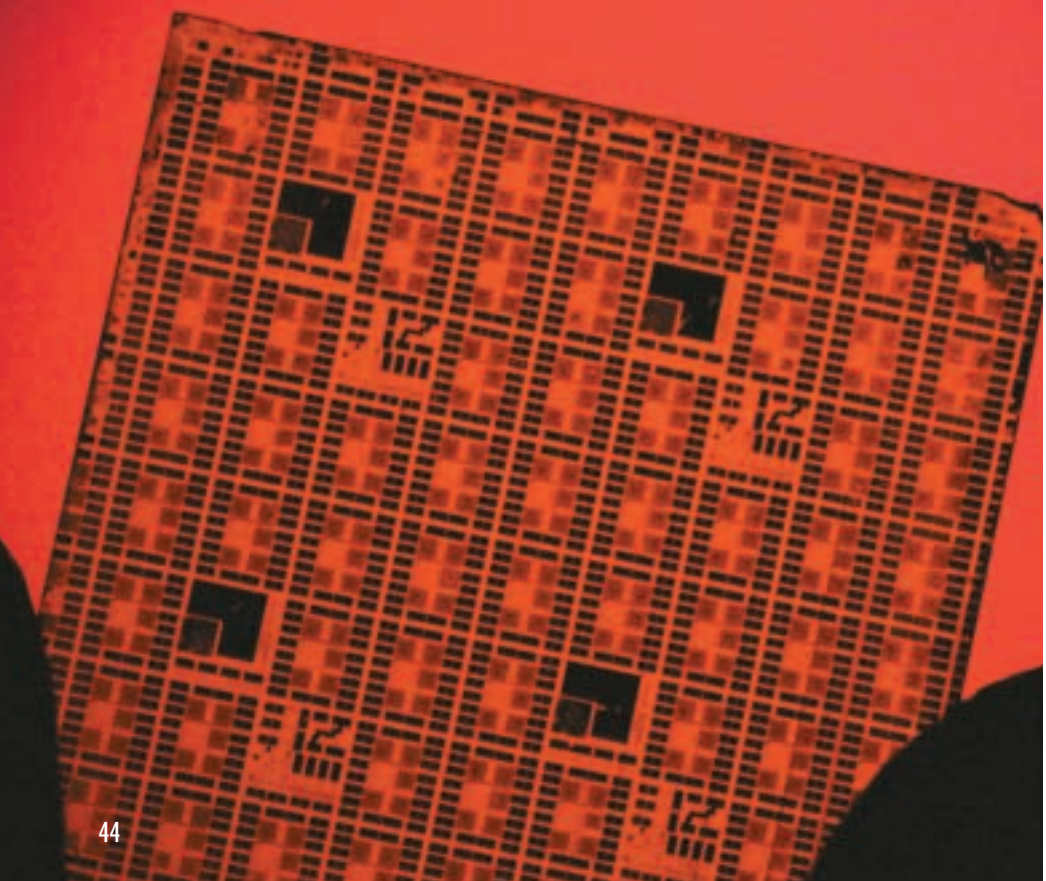
FPGAs — The Solution to Ultra-Deep Sub-Micron Design

With Xilinx FPGAs you can focus on your design function without being concerned with the tricky physical design issues caused by today's ultra-deep sub-micron device geometries.



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As device geometries decrease from 0.25µ to 0.13µ, the problems of substrate coupling, ground bounce, and interconnect crosstalk increase dramatically. ASIC designers who want to take advantage of these new device technologies are faced with a difficult task; they must create designs that are both logically correct and reliable within the specified environmental extremes. As device geometries decrease, it becomes much more difficult to produce reliable designs.

The FPGA Solution

The FPGA solution (consisting of both devices and software) assures you of a reliable design, because FPGAs are composed of a consistent architecture that has been tested over a long period of time, under real world conditions. Thus, FPGAs are guaranteed to operate exactly as specified, with very predictable interconnect delays, so you can spend more time on design optimization.

Substrate Coupling

Substrate coupling is a serious problem for either an ASIC or an FPGA. To guarantee performance, both ASIC and FPGA IC designers must use the best tools and models possible to accurately simulate the device, and have the means to automatically verify the design once it is ready for mask making.

Xilinx has developed proprietary automated techniques similar to those used by EDA vendor CadMOS (used in their SeismIC™ and PacifIC™ products for traditional DSM ASIC designs). We use these tools to automatically model and verify all of our FPGAs, which isolates you from this issue.

Substrate Bounce

Substrate bounce is caused by the switching of fast, high-current I/O transistors. It can cause double-clocking, as well as indeterminate and invalid logic states. The substrate bounce effects on Xilinx FPGAs are modeled precisely, and our designs are guaranteed to provide adequate isolation. For all of our FPGAs, Xilinx models and minimizes substrate noise in the design prior to making the device masks for fabrication.

Interconnect Crosstalk

Interconnect crosstalk between the tiny wires, on multiple metal layers, now requires a 3D field solver for extraction; anything less is not accurate enough to completely model the interconnections on the chip. Models must take into account the potential for crosstalk induced delay so that any possible user circuit will behave predictably and reliably, regardless of process and silicon variation. Xilinx IC designers perform extensive interconnect modeling using field modeling to ensure that our FPGAs do not have crosstalk problems.

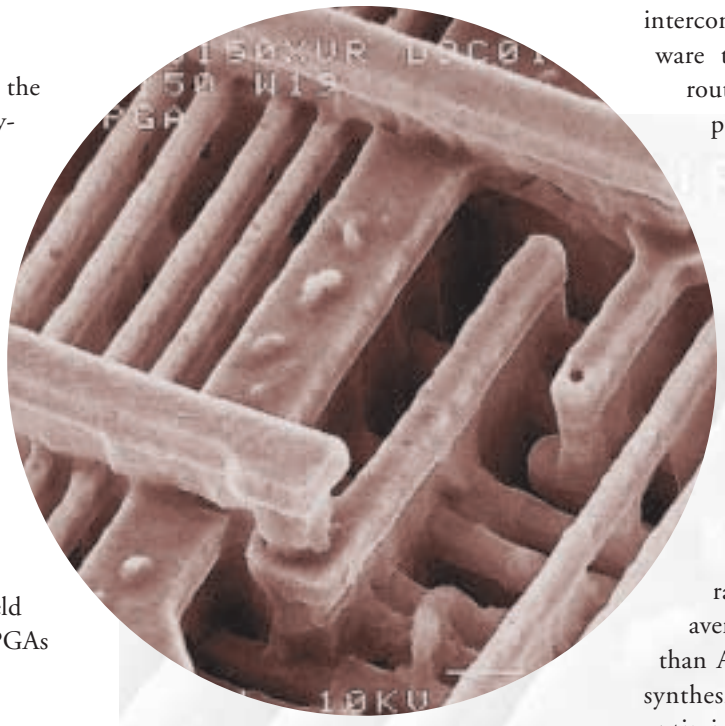
Device Fabrication

IC Designers must also model devices carefully to avoid yield problems, speed grading issues, and design failures. Xilinx manufactures millions of devices for each FPGA family, and the manufacturing process utilizes device monitors, test structures, and other process related structures that are measured on every wafer. The models are incrementally refined so that all process corners are modeled. The use of highly accurate device models enables Xilinx IC designers to rigorously verify and characterize all of our devices.

The combination of extensive and accurate modeling, simulations, and verification requires hundreds of engineer-years. Xilinx has made the investment and pre-engineered all of our devices so you don't have to worry about whether the silicon will work. ASIC IC designers must also expend the same effort, but often the expense is too high and resources are inadequate, resulting in designs that are not reliable.

The Software Solution

Using the current ultra-deep sub-micron design rules, interconnect delays account for approximately 75% of the path delays. Therefore, design modeling and timing closure become significant factors, and development tools are critical.



For FPGAs, interconnect delays have always been a significant portion of path delays because of the existence of switches in the routing paths. However, FPGAs have specific, fully characterized routing resources and, therefore, accurate delay models can be achieved using exhaustive empirical methods and functional analysis.

FPGA software tools are extremely mature in the area of handling interconnect delays. Therefore the ultra-DSM technology does not pose a new problem for FPGA place and route tools. Specifically, the delay estimation methods are mature and sophisticated resulting in accurate delay prediction. The placement and routing tools are smart enough to determine when to update the timing/slack information dynamically, based on changing interconnect delays during layout.

The newer Virtex and Spartan-II generation FPGAs, are co-developed by the Xilinx software and hardware teams. This process naturally results in a highly predictable architecture, and predictable interconnect delays. This allows the software to make correct placement and routing decisions early in the design process, even during the synthesis phase where there is maximum flexibility to influence the design performance.

The quality of the synthesis wireload models plays a key role in the timing predictability after synthesis. Advancements in FPGA synthesis technology (such as improved wire delay estimation by synthesis-driven placement tools) enable highly accurate timing predictability, and is on average 20% to 25% more accurate than ASIC technology. In addition, re-synthesis capabilities for critical path optimization reduce the number of design iterations for faster time to timing closure.

Conclusion

With FPGAs, you can now implement multi-million gate designs without being plagued by the DSM problems inherent in ASICs. Our advanced FPGA architectures shelter you from physical design issues such as crosstalk and ground bounce, and the latest synthesis and implementation software delivers timing predictability early in the design flow, giving you a significant reduction in design closure time, and a shorter time to market.