Xilinx Intellectual Property Solutions

The Most Comprehensive and Highest Quality Solution in the PLD Industry

The Xilinx Intellectual Property Solutions Division offers the best selection of Intellectual Property solutions for a wide variety of industries and applications. Xilinx Smart-IP Technology delivers high performance, flexibility, and predictability, with optimized cores that give you both reduced cost and faster time to market.

LogiCORE™ Products – Licensed and supported by Xilinx, LogiCORE products such as parameterizable DSP building blocks and memory cores are included with the Xilinx CORE Generator software which is a component of your Xilinx Foundation Series or Alliance Series software.

AllianceCORE™ Products – A cooperative program with third-party IP suppliers who sell and support their cores directly with Xilinx customers. AllianceCORE products must meet criteria that ensure they deliver value and performance in a Xilinx device.

Reference Design Alliance Program - Xilinx proactively supports development of third-party system-level Reference Designs to provide fully functional, modular designs, that offer considerable development time savings.

XPERTS Program – The worldwide XPERTS Program provides over 70 consultants certified in delivering turnkey system designs for the Xilinx architecture, including PCI designs, new design methodologies, system-level design, along with IP customization and integration.

IP Delivery Tools – The Xilinx CORE Generator™ enables cataloging and generation of parameterized cores that are high performance, predictable, and integrated with our system-level design reuse tools; the cores are provided in VHDL and Verilog behavioral description languages.

The IP Center Internet portal, provides access to the latest LogiCORE and AllianceCORE products and reference designs via Smart Search; you can easily find the IP that you need at www.xilinx.com/ipcenter. Advanced function cores are available for IP evaluation and can be purchased via the IP Center.

Design Reuse – Download the "Reuse Field Guide Methodology for FPGA and ASIC Designs." Then use the Xilinx IP Capture Tool to package your IP with simulation models, testbenches, and PDF or HTML files. Then, you can catalog and share your IP using the CORE Generator.

The REAL PCI 64/66 – Parameterizable PCI cores, reference designs, prototyping boards, education, and Xilinx PCI XPERTS combined with a proven design and guaranteed timing make Xilinx PCI the lowest risk solution in the market

The Xilinx DSP Solution – Our exclusive FPGA partnership with MathWorks enables you to create complex, high performance DSP designs in a familiar environment with huge time to market advantages. Xilinx and its partners offer a complete set of cores for high-performance low-cost DSP implementation that provide:

- **Xtreme Flexibility –** Distributed DSP resources (such as look up tables, registers, multipliers, memory) and segmented routing allow optimized implementation of algorithms. Plus you get all the traditional FPGA benefits:
  - RAM-based FPGA technology, for fast and easy design changes
  - Fast time to market, to give you a competitive advantage
  - Field upgradeable systems (using IRL™), for extended product lifecycle
- **Xtreme Productivity –** The industry's first System Generator for Simulink® bridges the gap between FPGA and conventional DSP design flows, and features:
  - Unique constraint-driven Filter Generator, for performance/cost optimization
  - Power estimator tool (Xpower™), for very low-power DSP implementations
  - Eleven optimized DSP algorithms (cores) that cut development time by weeks
  - New DSP features added to the ChipScope ILA tool, rapidly reduces hardware debugging time
- **Xtreme Performance -** Table 1 illustrates the amazing performance you can achieve with Xilinx DSP.

Table 1 - Extreme Performance

Function	Industry's Fastest DSP Processor Core	Xilinx Virtex-E -08	Xilinx VIRTEX
MACs per second - Multiply and accumulate - 8 x 8-bit	4.4 Billion	128 Billion	**600 Billion**
FIR Filter - 256-tap, linear phase - 16-bit data/coefficients	17 MSPS @ 1.1 GHz	160 MSPS @ 160 MHz	**180 MSPS** @ 180 MHz
FFT - 1024 point, complex data - 16-bit real and imaginary comp.	7.7 µs @ 800 MHz	41 µs @ 100 MHz	**<1 µs** @ 140 MHz