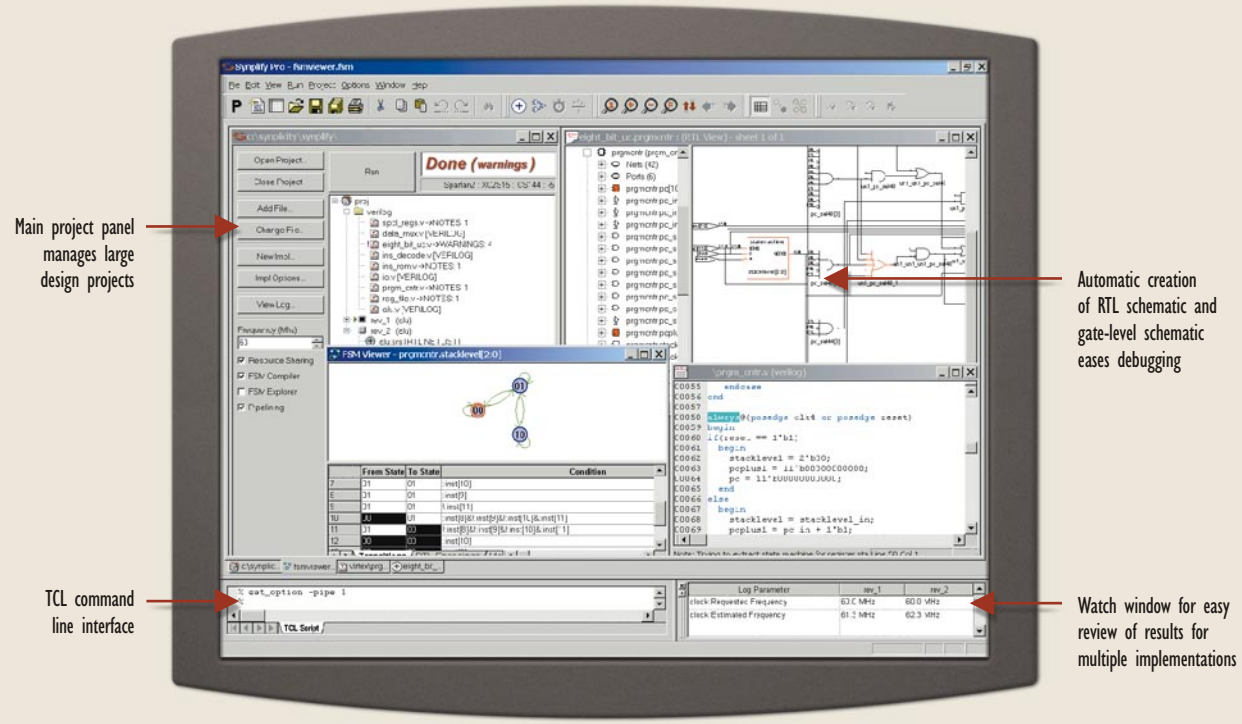
Synplify Pro™

A Powerful FPGA Synthesis Solution for Complex Programmable Logic Designs



High-performance FPGA synthesis

As system complexities advance, the complexity of programmable logic is following suit. High-density field programmable gate arrays (FPGAs) now contain millions of gates and operate at speeds in excess of 200 MHz. At this complexity, schedules, budgets and FPGA design tools all begin to feel the burden. Enter the Synplify Pro solution. It starts with all the features and lightning-fast runtimes that made the Synplify® product the industry's most popular and robust synthesis tool, and moves beyond with additional capabilities. Using the Synplify Pro solution, you can push the performance of complex FPGA designs while remaining comfortably on or ahead of schedule.

The Synplify Pro software addresses the unique requirements of complex FPGA projects. Where advanced project management features are required, such as controlling various implementations of a design, the Synplify Pro tool accommodates incremental design techniques, the integration of intellectual property and design re-use.

Proprietary retiming technology

The Synplify Pro product includes a powerful new capability for retiming circuits. By selecting a switch you can tell the tool to automatically move registers inside combinatorial logic in order to balance timing delay and improve circuit performance by as much as 20 percent. Retiming may be used on global level or selective level.

Visible results

A powerful graphical user interface displays multiple implementations including a project browser, a command line interface with an expanded TCL command set, a log watch window that displays synthesis results for multiple implementations simultaneously, plus batch mode operation.

Synplify Pro Features	Benefits
Proprietary B.E.S.T.™ Algorithms	Globally optimized designs in a fraction of the time required by traditional synthesis tools.
Integrated Module Generation and Mapping	Higher performing, area-efficient implementations of arithmetic/datapath functions.
Lightning-Fast Compile Times	Synthesizes even the largest design in minutes.
SCOPE® Multi-Level Design Constraints	Provides designer with complete control over the synthesis process.
Comprehensive Language Support	Supports Verilog, VHDL and mixed-language designs.
Language-Sensitive Editor	Automatic HDL syntax and synthesis checks for both Verilog and VHDL.
Intuitive Use Model w/ Intelligent Defaults	Be instantly productive with the tools.
Direct Synthesis Technology™ (DST™)	Leverages architecture-specific features to deliver the highest Quality of Results.
Automatic RAM Inferencing	Bypasses tedious hand instantiation of RAM.
Third-Party Tool Integration	Cross-probing with popular simulators and design entry tools.
FSM Explorer	Automatically finds and selects the best coding style option for the fastest performance.
Automatic Retiming	Moves registers automatically within combinatorial logic to balance delay & improve performance.
Graphical State Machine Viewer	Fast debugging and documentation for all state machines in your design.
Register Balancing for Pipelined Multipliers & ROMs	Automatic pipelining provides better throughput and faster circuit performance.
Probe Point Creation	Allows any signal to be tied to an external pin for testing without HDL code changes.
Generic Cross-Probing of Critical Paths	Cross-probe between the HDL Analyst tool and 3rd-party timing reports.
HDL Analyst® RTL Analysis & Debugging Tool	Instantly generates an RTL block diagram from HDL code; helps identify critical paths.

The powerful Synplify Pro synthesis solution

The Synplify Pro product delivers unmatched circuit performance with the most efficient area utilization for programmable logic designs. Like the Synplify product, Synplify Pro synthesis software is driven by Synplicity's proprietary Behavior Extracting Synthesis Technology® (B.E.S.T.), and also includes the Synthesis Constraint Optimization Environment® (SCOPE) multi-level, graphical constraints editor for a high level of control over your results.

Standard with the product is the powerful, easy-to-use HDL Analyst RTL graphical analysis and debugging tool. Providing instant graphical views of both high-level block diagrams and gate-level schematics linking back to the HDL source code, the HDL Analyst tool is an easier, faster way to debug HDL code for optimal performance.

FSM Explorer

An extremely useful feature of the Synplify Pro solution is the FSM Explorer, an enhancement to the Synplify product's unique finite state machine (FSM) compiler. FSM Explorer automatically finds state machines, then evaluates alternate coding styles and selects the one giving the best performance for the specified timing constraints. FSMs are displayed as bubble diagrams, providing an easy-to-read graphical representation of your results. This graphical view is especially useful for design debugging and documentation.

Pipelining

To dramatically increase performance with arithmetic operations, the Synplify Pro product will automatically move registers inside ROMs and multipliers to create pipeline stages.

The Amplify® Physical Optimizer™

For the best FPGA performance possible, the Amplify Physical Optimizer is an option for the Synplify Pro tool. The first and only physical synthesis solution for FPGA design, the Amplify tool uses RTL graphical physical constraints with innovative algorithms that simultaneously employ placement and logic optimization for up to 40% faster circuit performance than logic synthesis alone.

Design tool interfaces

The Synplify Pro tool interfaces to simulators such as NC-Verilog, NC-VHDL, Active-HDL, ModelSim and SpeedWave, plus many popular, high-level graphical entry tools. It integrates with place & route tools from Actel, Altera, Atmel, Cypress, Lattice, Lucent, QuickLogic, Triscend, and Xilinx.

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