Agenda

- Introduction
  - Market trend and application
    - 1394 Market Analysis Data
    - 1394 and industry
    - Applications
- Technology
  - What is 1394?
  - Why 1394?
  - Applications
  - 1394 Protocol
  - PHY
  - Link Layer
  - Transaction Layer
  - 1394 Operation
  - Bus Management
  - Cable and Connection
  - Architecture
  - Topology
- Other Technologies
  - USB
  - DVI
- 1394 In Home Networking
- Xilinx Value
- Alliances
- Summary

Why IEEE 1394?

- A digital interface
  - There is no need to convert digital data into analog and tolerate a loss of data integrity
  - Transferring data @ 100, 200, 400 Mbps (Cable)
  - Transferring data @ 12.5, 25 or 50 Mbps (Backplane)
- Physically small
  - The thin serial cable can replace larger and more expensive interfaces

Why IEEE 1394?

- Easy to use
- There is no need for terminators, device IDs, or elaborate setup
- Hot pluggable
  - Users can add or remove 1394 devices with the bus active
- Inexpensive
  - Priced for consumer products
- Scaleable architecture
  - May mix 100, 200, and 400 Mbps devices on a bus

Why IEEE 1394?

- Flexible topology
  - Support of daisy chaining and branching for true peer-to-peer communication
- Non-proprietary

IEEE 1394b

- 1394b is a significant enhancement to the basic 1394 specification that enables:
  - Speed increases to 3.2 Gbps
  - Supports distances of 100 meters on UTP-5, plastic optical fiber, and glass optical fiber
  - Significantly reduces latency times by using arbitration pipelining
- It is fully backwards compatible with the current 1394 and 1394a specifications

New Extensions (1394b)

- Gigabit speeds for cables
- 100Mb for backplane implementations
- Longer distance cables using copper wire and fiber
- A/V command and control protocols
- 1394 to 1394b bus bridges
- IEEE 1394 gateways to communication interfaces, such as ATM

IEEE 1394 Standards Update

- 1394-1995
  - Supports up to 400 Mbps Links and PHYs
  - 6 pin cables
- 1394a (1998)
  - Power management clean up
  - Cable power specification in flux
- Open Host Controller Interface (1998)
  - Ultimate goal is a single driver for OS support
- 1394b (1999)
  - Could be a legitimate storage I/O at 800 Mbps

1394 Based Applications

- Digital camcorders and VCRs
- Direct-to-Home (DTH) satellite audio/video
- Cable TV and MMDS (microwave) set-top boxes
- DVD Players
- Video Games
- Home Theater
- Home Networks

1394 Based Applications

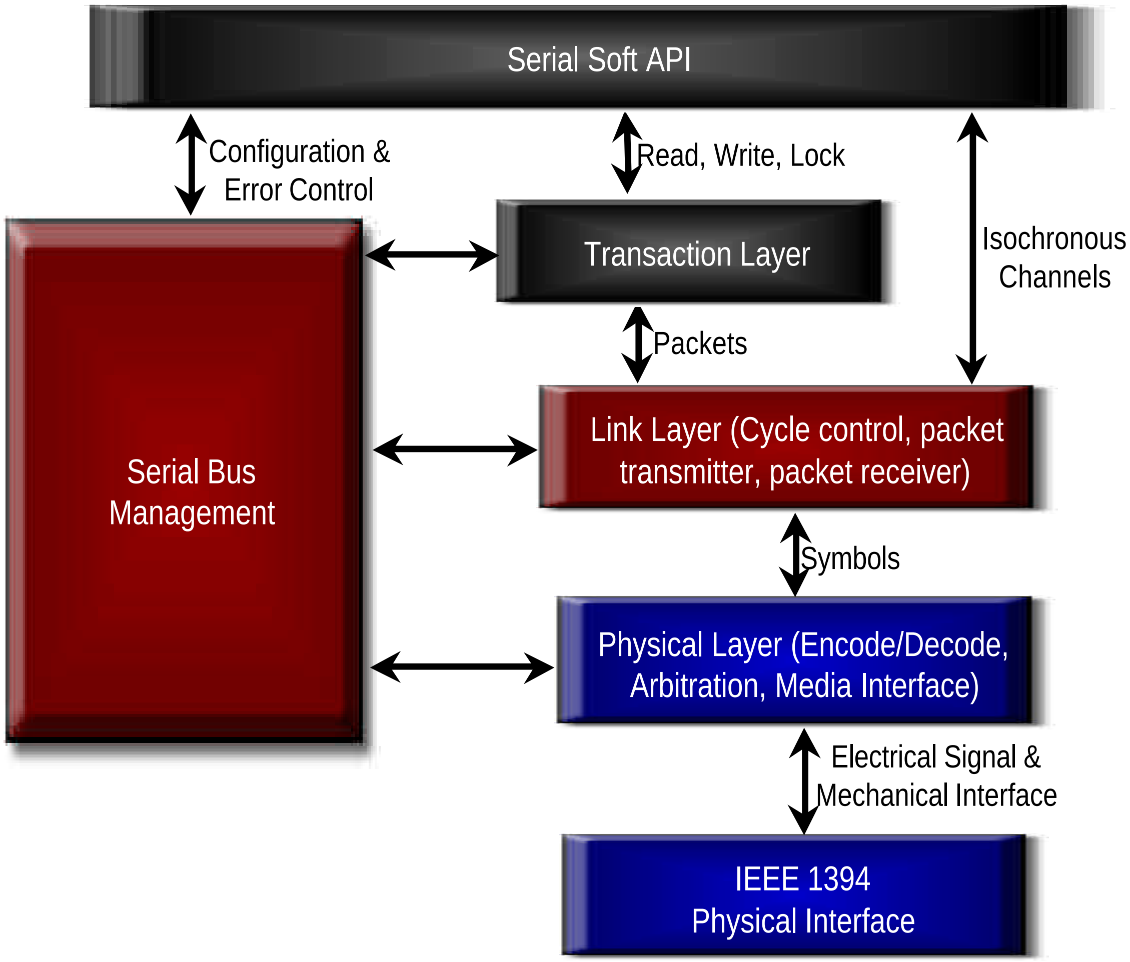
- Musical synthesizers/samplers with MIDI and digital audio capabilities
- Digital audio tape (DAT) recorders, mixers, hard-disk recorders, video editors, etc.
- Professionals and affluent consumers Digital Video (DV) applications
- Professional video equipment
- Fixed and removable PC disk drives

1394 Based Applications

- PC-to-PC networking and PC peripheral component sharing
- Printers for video and computer data
- Digital cameras and videoconferencing cameras
- Industrial

IEEE 1394 Protocol

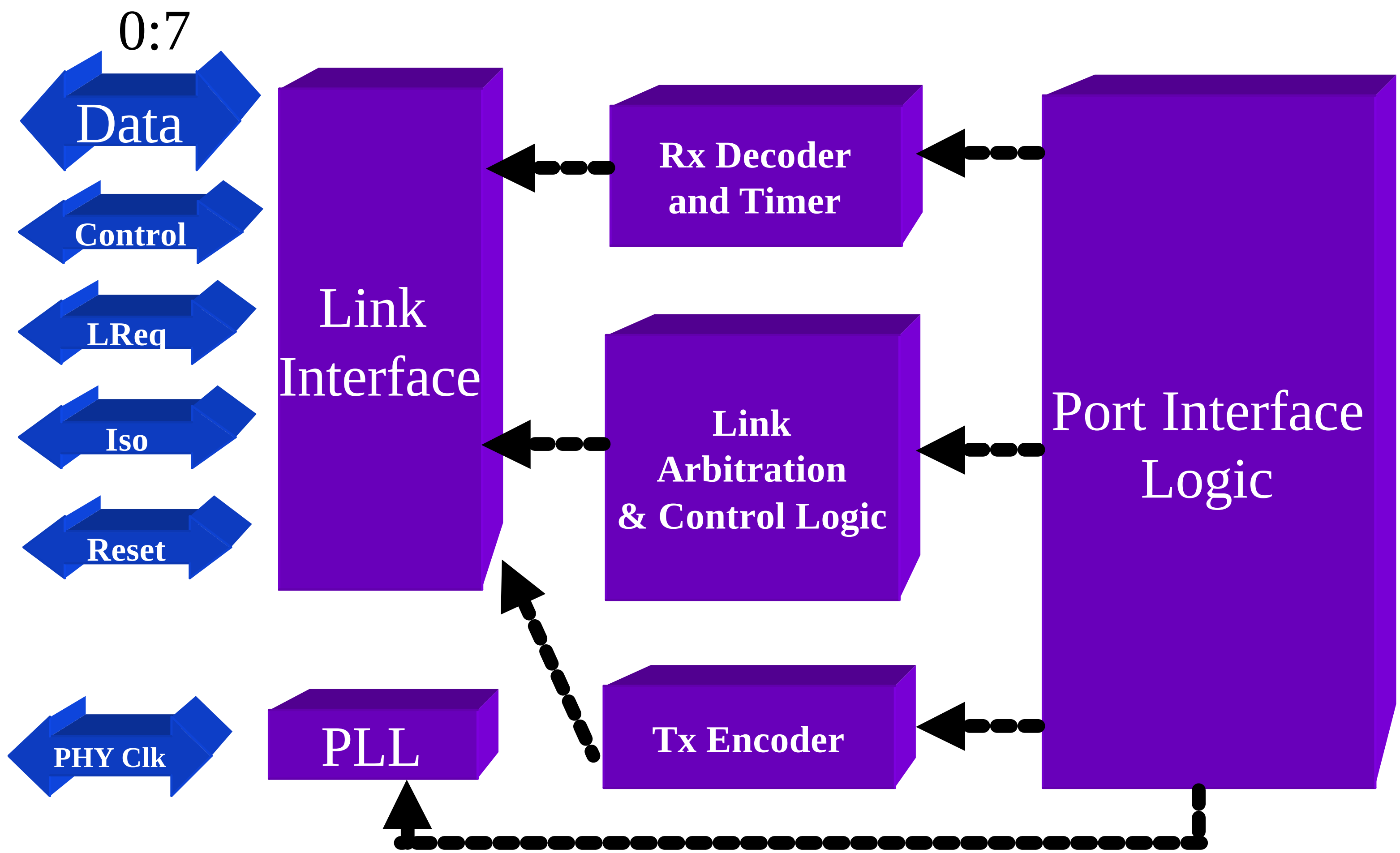
IEEE 1394 Protocol Stack



1394 PHY Layer

- The Physical layer provides the initialization and arbitration services
  - It assures that only one node at a time is sending data
- The physical layer of the 1394 protocol includes:
  - The electrical signaling
  - The mechanical connectors and cabling
  - The arbitration mechanisms
  - The serial coding and decoding of the data being transferred or received
  - Transfer Speed detection

1394 PHY


0:7
Data
Control
LReq
Iso
Reset
PHY Clk
Link Interface
PLL
Rx Decoder and Timer
Link Arbitration & Control Logic
Tx Encoder
Port Interface Logic

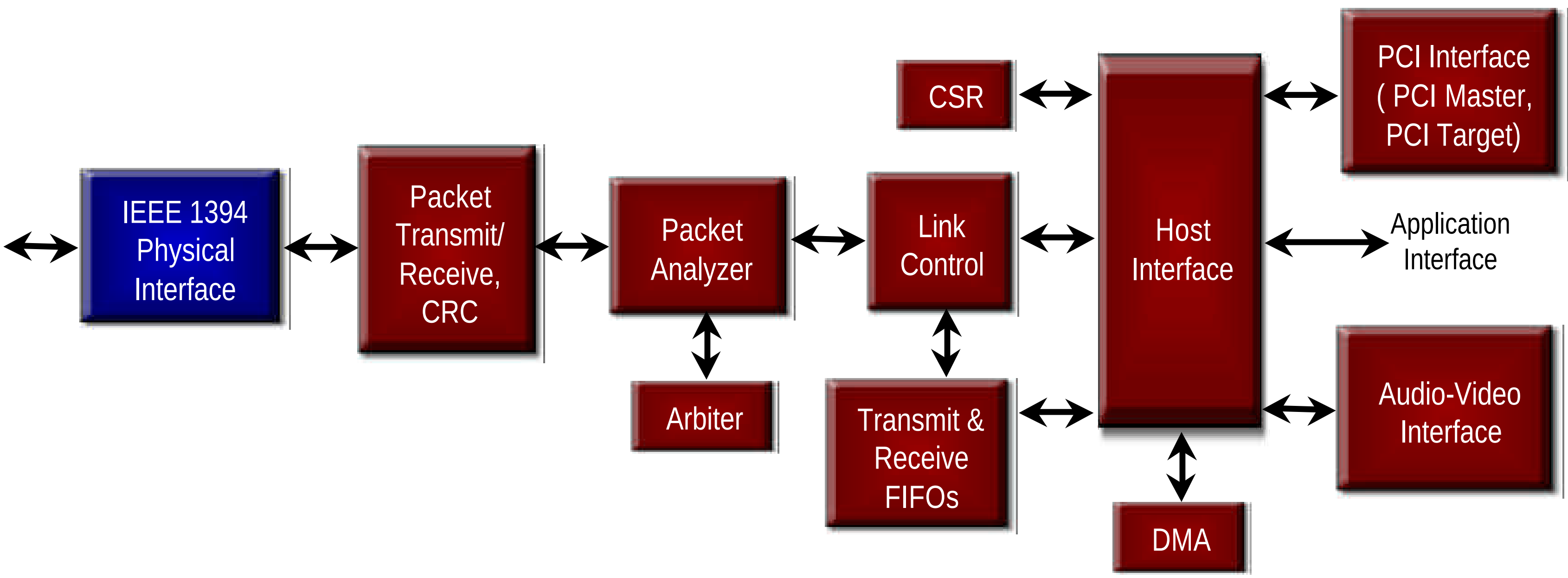
Physical layer Controller Products

Physical Layer Controllers Manufacturer	Part Number	Description
Fujitsu Microelectronics	MB8661x	Combined link/PHY core & ICs
IBM	IBM21S85xPFD IBM21S760PFD	400Mbps 1- and 3-port devices 200Mbps 1- and 3-port devices
Innovative Semiconductor	SL75x	Physical layer cores
Philips Semiconductor	PDI1394P11	Physical layer IC
Macro Designs		Physical layer cores
Phoenix Technologies	VirtualLink	100, 200, and 400Mbps 1394a-compatible cores
Sand	1394 CPHY	1394 cable physical layer core
Symbios (LSI)	SYM13FW403	1394 cable PHY interface IC
NEC	uPD72850	3-port PHY IC
Texas Instruments	TSB11C01 TSB11LV01 TSB14C01A TSB21LV03A TSB41lV0x	Up to 400Mbps PHY ICs
Sony	CXD1944R	3-Port 200Mbps PHY IC

Link Layer

- Gets data packets on and off the wire
- Does error detection and correction
- Does retransmission
- Handles provision of cycle control for Isochronous channels
- The Link layer supplies an acknowledged datagram to the Transaction layer
  - A datagram is a one-way data transfer with request confirmation

IEEE 1394 Link Controller



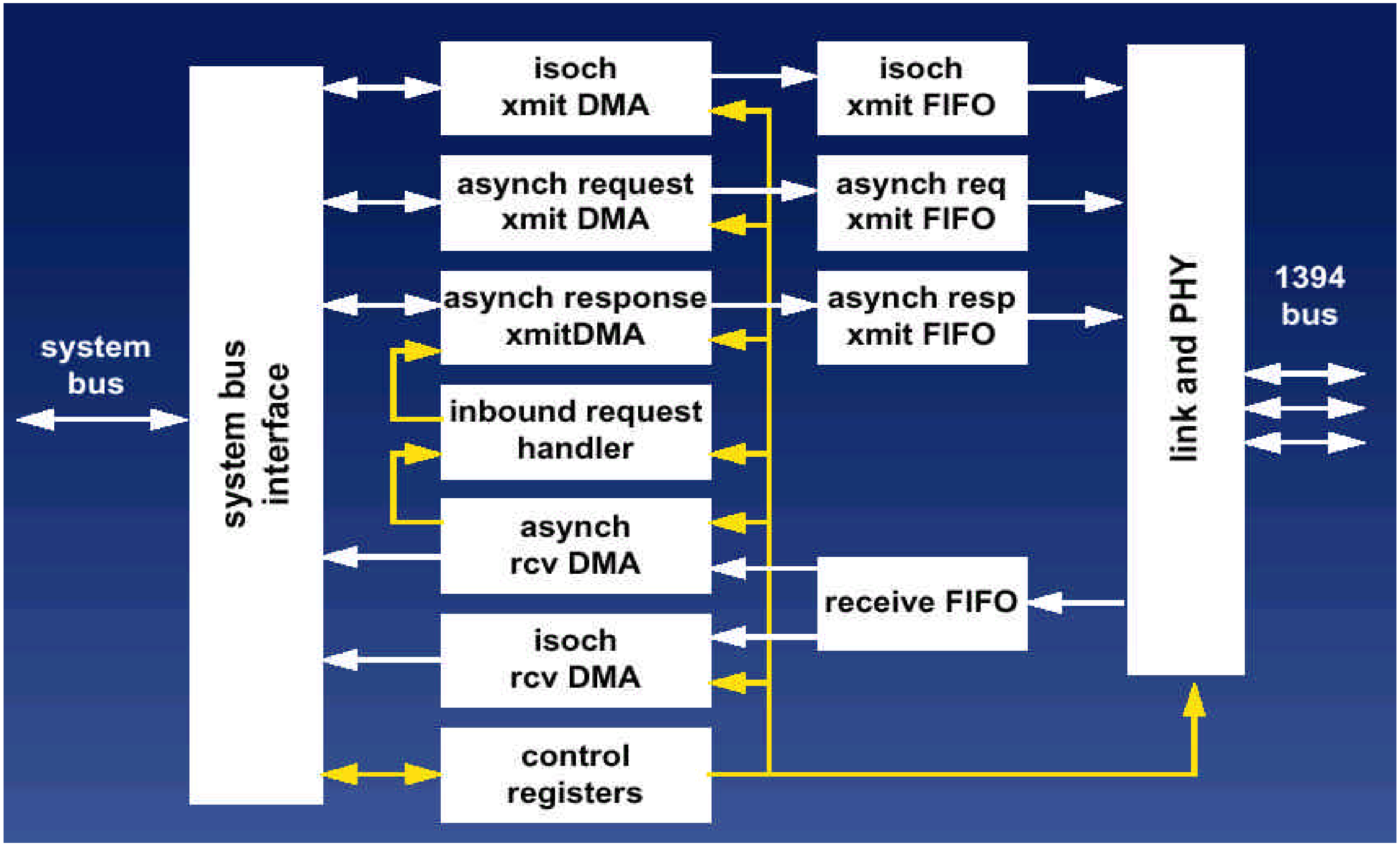
Link Layer Controller Products

Link Layer Controllers Manufacturer	Part Number	Description
Fujitsu Microelectronic	MB8661x	Combined link/PHY core & ICs
IBM	IBM21S650PF IBM21S550PFB	A PCI-based link layer controller Generic bus interface link layer controller
Innovative Semiconductor	SL75x	Link layer cores
Philips Semiconductor	PDI1394L11	A/V link layer controller
Phoenix Technologies	Virtual Link 1394a	Compatible link layer cores
Sand	1394 Device Controller	1394 link layer core
LSI	Sand Microelectronics	1394 Link Layer
NEC	uPD728xx	OHCI link layer IC (some integrate PHY)
Texas Instruments	TSB12LV21B TSB12LV22 TSB12LV31	Lynx HCI (PCI) IC OHCI (PCI) IC General-purpose bus interface IC
Sony	CXD1940R	AV protocol support

Transaction Layer

- Implements the request-response protocol
- This protocol is required to conform to:
  - ISO/IEC 13213 [ANSI/IEEE Std 1212, 1994 Edition] Standard Control
  - Status Register (CSR) Architecture for Microcomputer Buses
- Conformance to ISO/IEC 13213:1994
  - Minimizes the amount of circuitry required by1394 ICs to interconnect with 1212-standard parallel buses, such as the PCI bus

IEEE 1394 Host Controller



Courtesy of Apple

IEEE 1394 Operation

IEEE 1394 Operation

- Isochronous Transfers
  - Isochronous transfers are always broadcast in a one-to-one or one-to-many fashion
  - No error correction nor retransmission is available for Isochronous transfers
  - Up to 80% of the available bus bandwidth can be used for Isochronous transfers
  - The delegation of bandwidth is tracked by a node on the bus
  - Isochronous channel IDs are transmitted followed by the packet data
  - The receiver monitors the incoming data's channel ID and accepts only data with the specified ID

IEEE 1394 Operation

- Asynchronous Transfers
  - Asynchronous transfers are targeted to a specific node with an explicit address
  - They are not guaranteed a specific amount of bandwidth on the bus
  - They are guaranteed a fair shot at gaining access to the bus when asynchronous transfers are permitted
  - Asynchronous transfers are acknowledged and responded to
    - This allows error-checking and retransmission mechanisms to take place

IEEE 1394 Operation

- Isochronous transfers are the best choice for sending time-critical, and error-tolerant data
  - Video or Audio stream
- If the data isn't error-tolerant, such as a disk drive, then asynchronous transfers are preferable

Bus Management

- The Bus Manager must collect the self-id packets and create the topology and speed maps from them
- Bus management involves the following three services:
  - A Cycle Master that broadcasts cycle start packets (required for Isochronous operation)
  - An Isochronous Resource Manager, if any nodes support Isochronous communication
  - An optional Bus Master

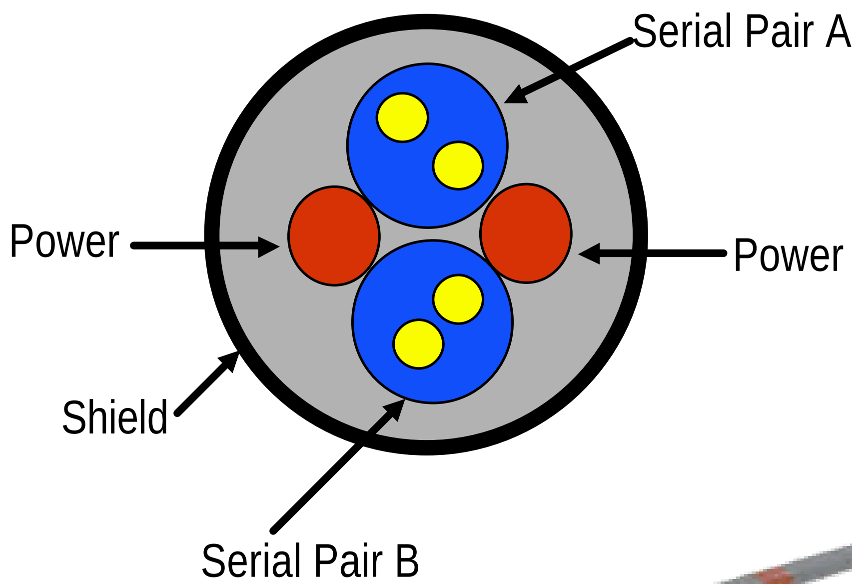
Bus Management

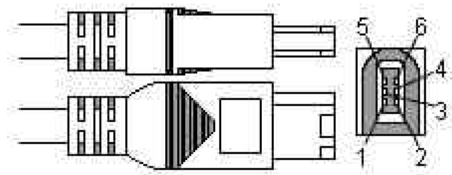
- The structure of the bus is determined on bus reset
  - Node IDs (physical addresses) are assigned to each node
  - Arbitration occurs for Cycle Master, Isochronous Resource Manager, and Bus Master nodes
- Serial bus management in portable consumer products is handled by a microprocessor designed to minimize battery power consumption
  - Most battery-operated 1394 gear is expected to run at S100 speed for power conservation

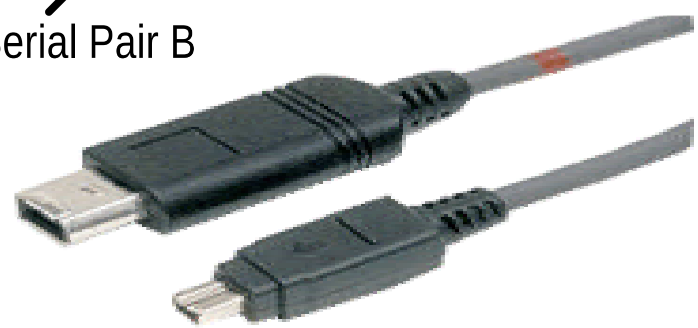
IEEE 1394 Cabling

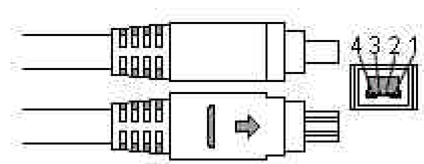
- It can connect up to 63 devices @ transfer rate of 400Mbps
- Is "hot-pluggable" and PnP
- A 1394 cable can be up to 15 feet in length
- The 6-pin connectors have two data wires and two power wires for devices which derive their power from the 1394 bus
- Data-only cables use one 6-pin and one 4-pin connector or two 4-pin connectors

Cable









IEEE 1394 Architecture (Bus Categories)

- Backplane bus
  - Supplements parallel bus structures by providing an alternate serial communication path between devices plugged into the backplane.
- Cable bus
  - Is a "non-cyclic network
    - Devices can not be plugged together to create loops
  - The networks has finite branches, consisting of bus bridges and nodes
  - 16-bit addressing provide for up to 64K nodes in a system
  - Up to 16 cable hops are allowed between nodes, thus the term finite branches

IEEE 1394 Architecture (Bus Categories)

- A bus bridge serves to connect busses of similar or different types
- A bus bridge also would be used to interconnect a 1394 cable and a 1394 backplane bus
- Six-bit Node_IDs allow up to 63 nodes to be connected to a single bus bridge
- 10 bit Bus_IDs accommodate up to 1,023 bridges in a system.

IEEE 1394 Architecture

- Each node usually has three connectors
- Up to 16 nodes can be daisy-chained through the connectors
  - Standard cables up to 4.5 m in length for a total standard cable length of 72 m.
- Additional devices can be connected in a leaf-node configuration
- Physical addresses are assigned on:
  - Bridge power up(bus reset)
  - Whenever a node is added or removed from the system, either by physical connection/disconnection or power up/down

Connection Steps

- Step 1: Physical connection between two nodes
  - Triggers serial bus configuration
- Step 2: Bus Reset
  - Forces all nodes to their initialized state
  - All bus topology information is cleared
- Step 3: Tree Id
  - Transforms a simple net topology into a tree topology
- Step 4: Self ID
  - Assigns physical node numbers or IDs
  - Exchanges speed capabilities with neighbors
- Step 5: Arbitration

Connection Steps (Reset)

- Reset is signaled by a node driving both TPA and TPB to logic 1.
  - A logic 1 will always be detected by a port, even if its bi-directional driver is in the transmit state.
- When a node detects a reset, it will propagate this signal to all of the other ports that this node supports.
- The node then enters the idle state for a given period of time to allow the reset indication to propagate to all other nodes on the bus.
- Reset clears any topology information within the node

Connection Steps (Tree identification)

- Defines the bus topology.
- After reset, all leaf nodes present a Parent_Notify signaling state on their data and strobe pairs.
- When a branch node receives the Parent_Notify signal on one of its ports, it marks that port as containing a child, and outputs a Child_Notify signaling state.
  - The ports marked with a “P” indicate that a device which is closer to the root node is attached to that port.
  - The port marked with a “C” indicates that a node farther away from the root node is attached.

Connection Steps (Self Identification)

- Self identification consists of:
  - Assigning physical IDs to each node on the bus
  - Having neighboring nodes exchange transmission speed capabilities
  - Making all of the nodes on the bus aware of the topology that exists
- The self identification phase begins with the root node sending an arbitration grant signal to its lowest numbered port.
- The root node will then continue to signal an Arbitration Grant signal to its lowest numbered port.

Connection Steps (Arbitration)

- Immediately following the cycle start packet, devices that wish to broadcast their Isochronous data may arbitrate for the bus.
  - Cycle is a time slice with a nominal 125µs period
- Arbitration consists of signaling a designated parent node a wish to gain access to the bus.
- The parent nodes in turn signal their parents and so on, until the request reaches the root node.
- The closest device to the root node wins the arbitration.

Topology

- The 1394 protocol is a peer-to-peer network with a point-to-point signaling environment
  - A specific host isn't required
    - Digital camera could easily stream data to both the digital VCR and the DVD-RAM without any assistance from other devices on the bus
- Nodes on the bus may have several ports on them
  - Each of these ports acts as a repeater, retransmitting any packets received by other ports within the node

Topology

- Configuration of the bus occurs automatically whenever a new device is plugged in
- During system initialization, each node in a 1394 bus carries out :
  - A process of bus initialization
  - Tree identification
  - Self-identification
- A 1394 bus appears as a large memory-mapped space with each node occupying a certain address range

Topology

- The memory space is based to the IEEE 1212 Control and Status Register (CSR) Architecture
  - With some extensions specific to the 1394 standard
- Device addressing is 64 bits wide partitioned as:
  - 10 bits for network Ids
  - 6 bits for node Ids
  - 48 bits for memory addresses
- Each node supports up to 48 bits of address space (256 Tera Bytes)

Topology

- Each bus can support up to 64 nodes
  - The 1394 serial bus specification supports up to 1,024 buses
- The topology of a 1394 system can be:
  - Daisy chain
  - Tree
  - Star
  - Or a combination of these
- 1394 can connect devices directly without the intervention of a computer