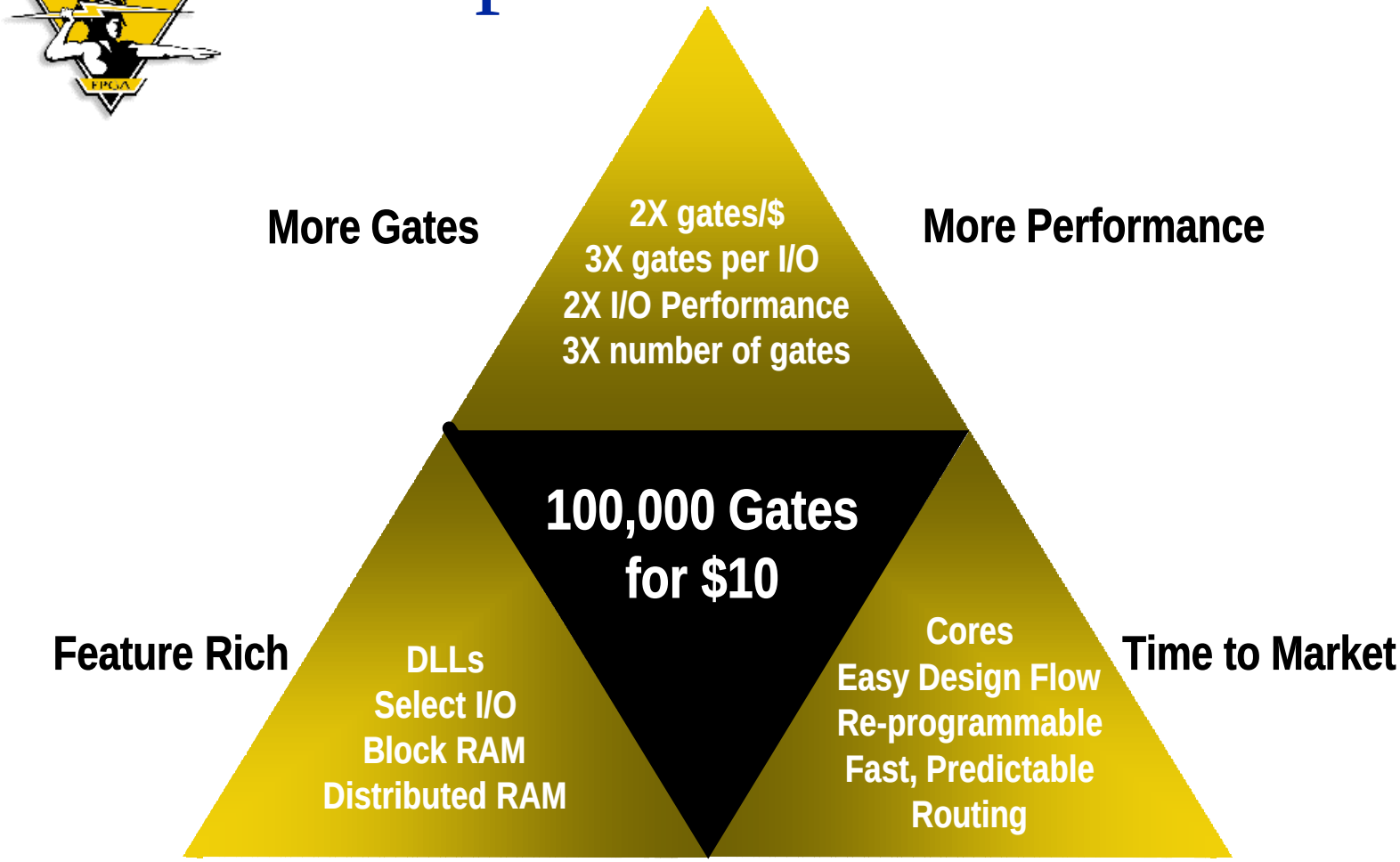
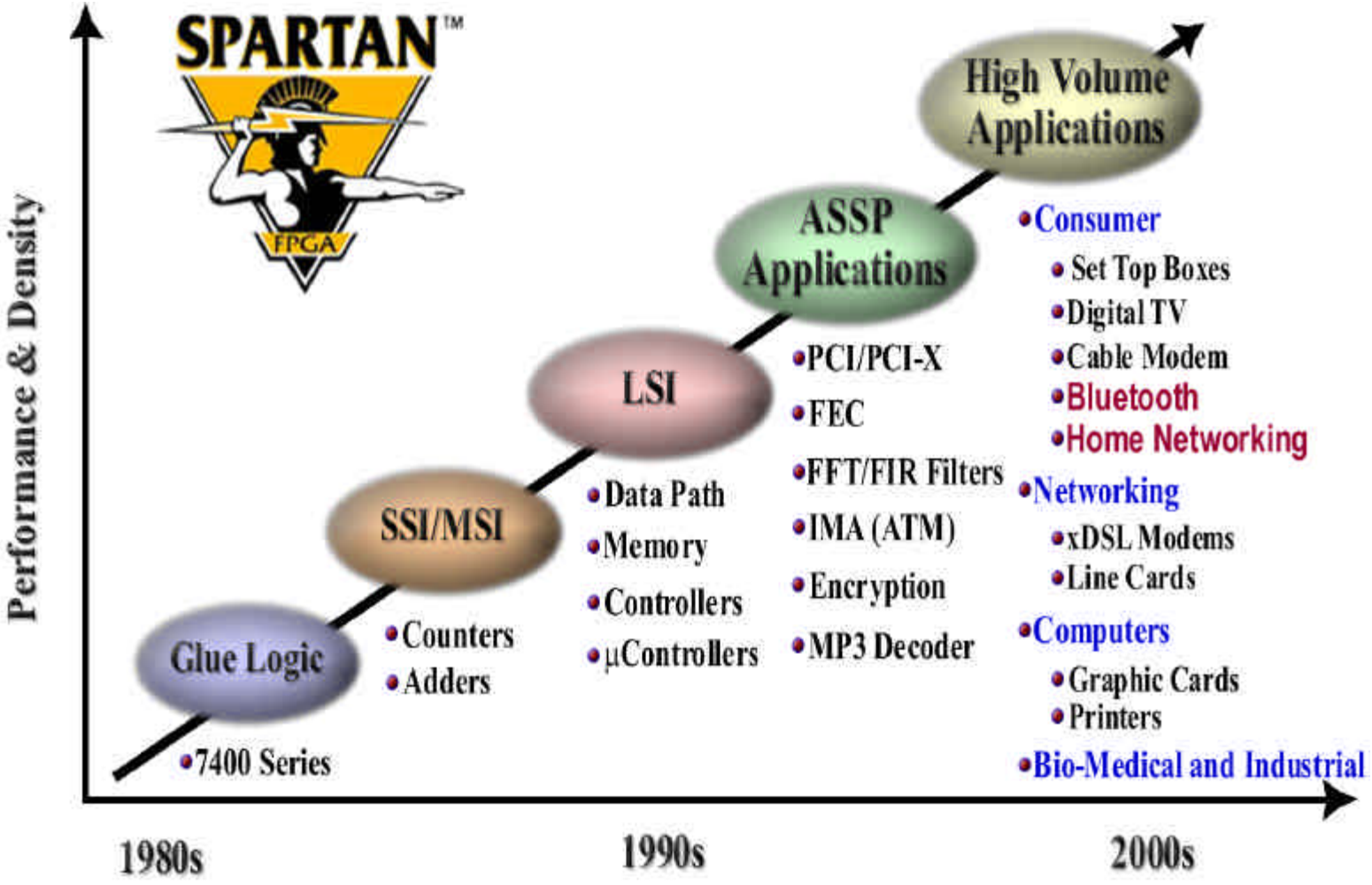
Spartan-II: Extending the Spartan Series



Programmable ASIC/ASSP Replacement!

FPGA Application Trends



Programmable ASIC/ASSP Replacement!

Spartan-II Feature Rich For Set-Top Box Solutions

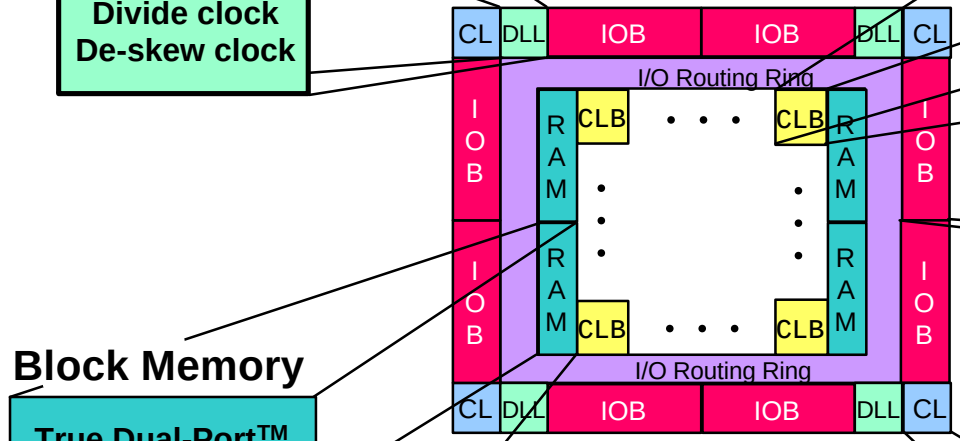
Delay Locked Loop (DLL)

Clock Management:

Multiply clock
Divide clock
De-skew clock

Configurable Logic Blocks (CLB)

Configurable Logic Block Array and Distributed RAM



Select I/O™ Technology

Chip to Backplane
PCI 33MHz 3.3V
PCI 33MHz 5.0V
PCI 66MHz 3.3V
GTL, GTL+, AGP
Chip to Memory
HSTL-I, HSTL-III
HSTL-IV
SSTL3-I, SSTL3-II
SSTL2-I, SSTL2-II
CTT
Chip to Chip
LVTTL, LVCMOS

Block Memory

True Dual-Port™ 4K bit RAM

4Kx1
2Kx2
1Kx4
512x8
256x16

"The Spartan-II family, in our opinion, may be the closest that any FPGA has come to being at a low-enough price to compete against an ASIC"
--Dan Niles, Robertson Stephens

Spartan-II Core Support

- BaseBLOX Basic Functions
  - Arithmetic (adders, counters, multipliers, etc.)
  - On-Chip memory (single port, dual port, FIFO, etc.)
- LogiCORE Support
  - PCI
  - DSP Functions
- AllianceCORE Support
  - Microprocessor peripherals
  - Microcontrollers
  - Memory controllers (SDRAM, QDR SRAM)
  - Communications
    - ATM (DSS, DSD, UTOPIA, etc.)
    - Ethernet (MAC)
    - Error correction (Reed-Solomon, Viterbi)
    - Telecom (HDLC, XF-HDLC, XF-MOD-DVB, etc.)

Spartan-II - System Integration